

# ***NDU00/NDU10***

***Streamline-S 11.6"***

***Streamline-M 13.3"***

## **LA-6031P REV 1.0 Schematic**

**Intel Arrandale SFF/IBEX PEAK**

**2010-04-12 Rev 1.0**

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# Compal Confidential

Model Name :NDU00/NDU10

File Name : LA-6031P

Clock Generator  
SLG8SP587VTR  
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Mobile  
Arrandale CPU  
BGA 1288pins

Memory BUS(DDRIII)  
Dual Channel

200pin DDRIII-SO-DIMM X2  
BANK 0, 1, 2, 3  
page 11, 10

1.5V DDRIII 800/1066 MT/s

page 5, 6, 7, 8, 9

FDI X8  
2.7GHz

DMI X4  
2.5GHz

USB/B  
USB port 0,1  
page 30

BT conn  
USB port 5  
page 25

3G  
USB port 12  
page 26

Int. Camera  
USB port 11  
page 12

LCD Conn.  
page 12

LVDS-A

CRT (Sub-board)  
page 13

RGB

HDMI Conn.  
page 14

HDMI Level Shifter  
page 14

DDP-C

3G  
PCIe port 4  
page 26

PCIe 1x  
1.5V 2.5GHz(250MB/s)

RJ45+Transformer (Sub-board)  
page 27

RTL8105E 10/100M  
PCIe port 1  
page 27

PCIe 1x  
1.5V 2.5GHz(250MB/s)

Cardreader conn.  
page 28

CardReader JMB389  
PCIe port 5  
page 28

PCIe 1x  
1.5V 2.5GHz(250MB/s)

Intel Ibex Peak

FCBGA1071

page 15~23

USB  
5V 480MHz

USB  
5V 480MHz

PCIe 1x  
1.5V 2.5GHz(250MB/s)

SATA port 1  
5V 3GHz(300MB/s)

SATA port 5  
5V 3GHz(300MB/s)

USB port 3  
5V 480MHz

PCIeMini Card  
WiMax  
USB port 13  
page 26  
PCIeMini Card  
WLAN  
PCIe port 2  
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SATA HDD0  
page 24

eSATA  
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USB  
USB port 3  
page 24

SPI

LPC BUS  
3.3V 33 MHz

HD Audio  
3.3V/1.5V 24MHz

Power/B

page 33

RTC CKT.

page 15

DC/DC Interface CKT.

page 34

Power Circuit DC/DC

Page 7~8

SPI ROM  
page 15

Debug Port  
page 32

ENE KB926 E0  
page 31

Touch Pad  
page 33

Int.KBD  
page 25

EC ROM  
page 32

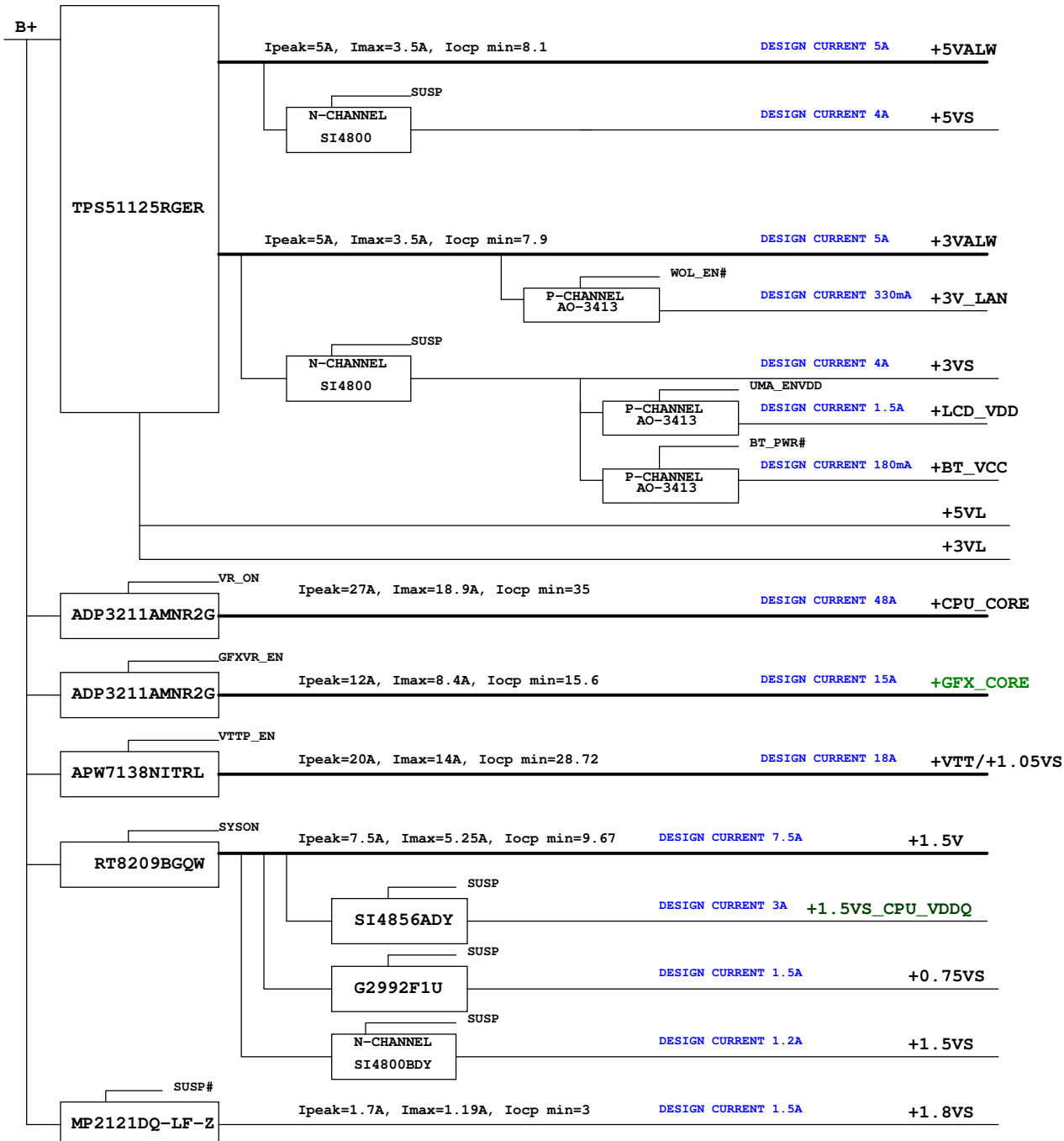
HDA Codec  
ALC259  
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Audio sub-board  
page 30

SPK CONN  
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NSWAA Liverpool Intel Arrandale  
NTWAA Sunderland Intel Arrandale



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Voltage Rails

( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	main	2nd
						R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

EC SM Bus1 address

EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011x b	+3VS	Gensor	
			+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

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5V

TP SKTOCC# M71

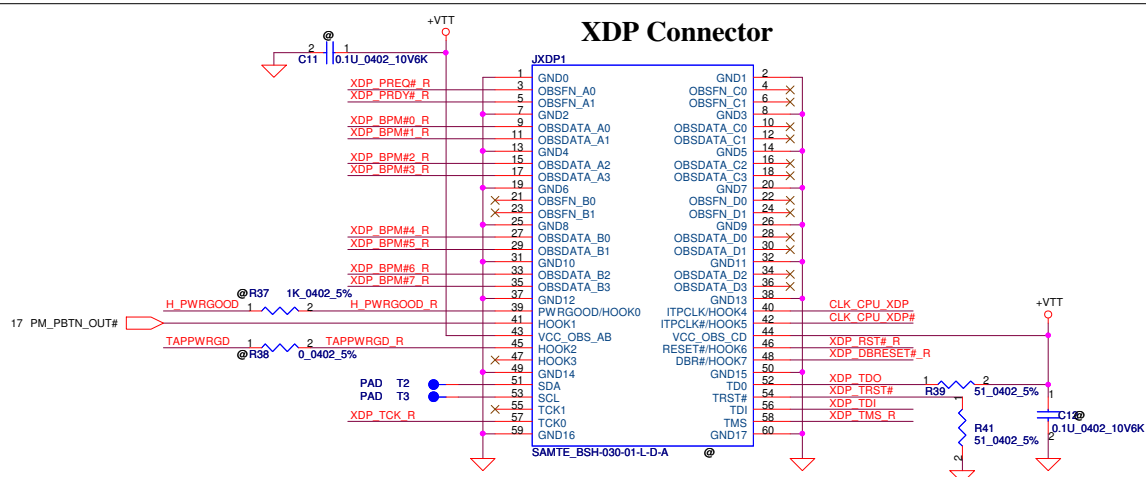
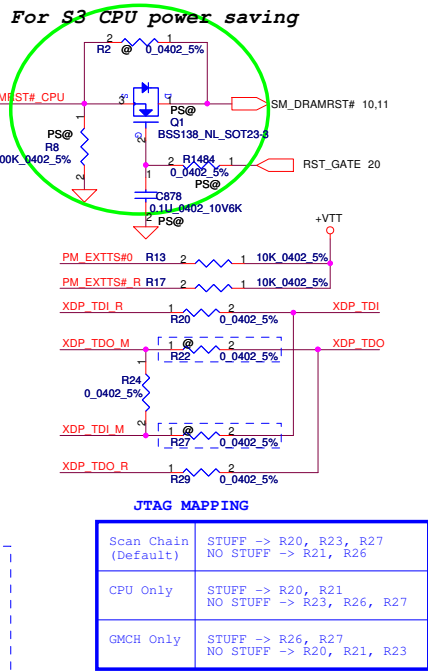
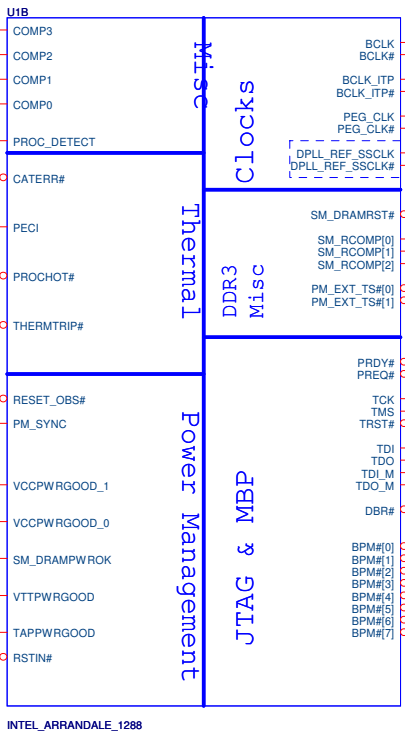
R1 20.0402\_1% H\_COMP3 AD71

R2 20.0402\_1% H\_COMP2 AC70

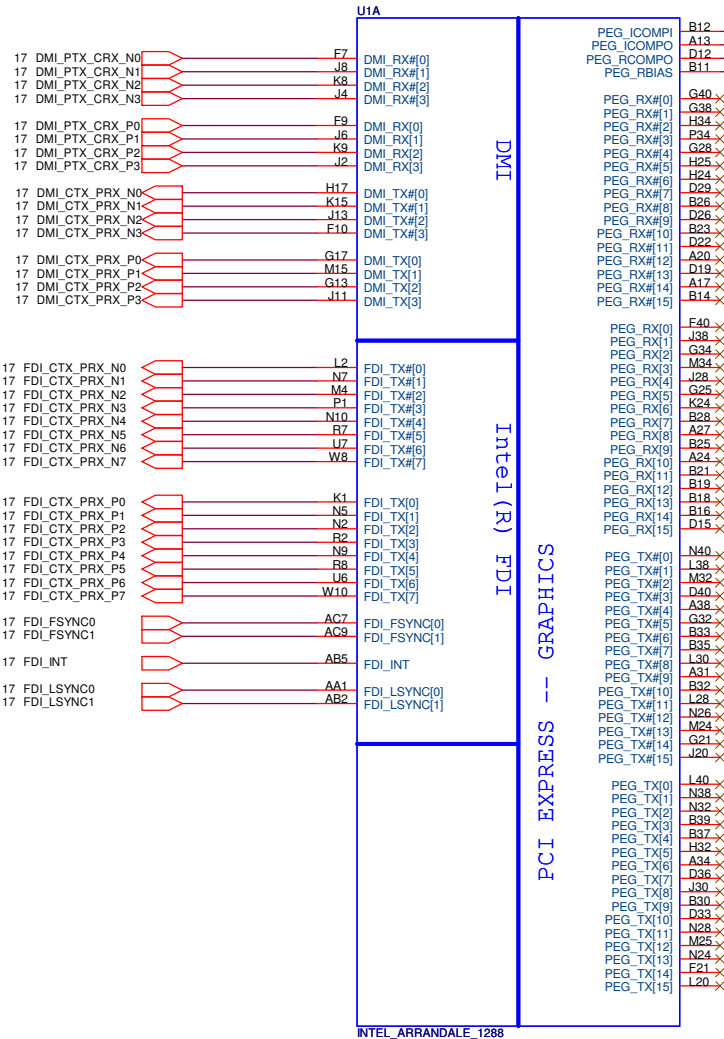
R3 20.0402\_1% H\_COMP1 AD69

R4 49.9.0402\_1% H\_COMP0 AE66

5V



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### CFG Straps for PROCESSOR

**CFG0** R93 1 2 @3.01K 0402 1%

PCI-Express Configuration Select

CFG0 1: Single PEG  
0: Bifurcation enabled

Not applicable for Clarksfield Processor

**CFG3** R79 1 2 @3.01K 0402 1%

CFG3-PCI Express Static Lane Reversal

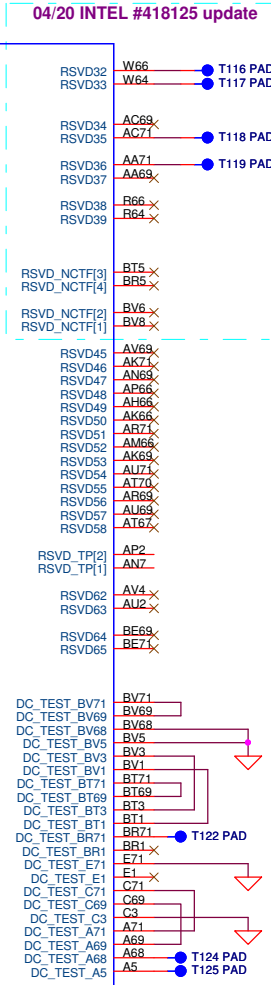
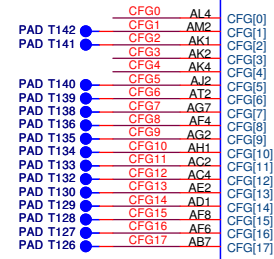
CFG3 1: Normal Operation  
0: Lane Numbers Reversed  
15 -> 0, 14 -> 1, .....

**CFG4** R272 1 2 3.01K 0402 1%

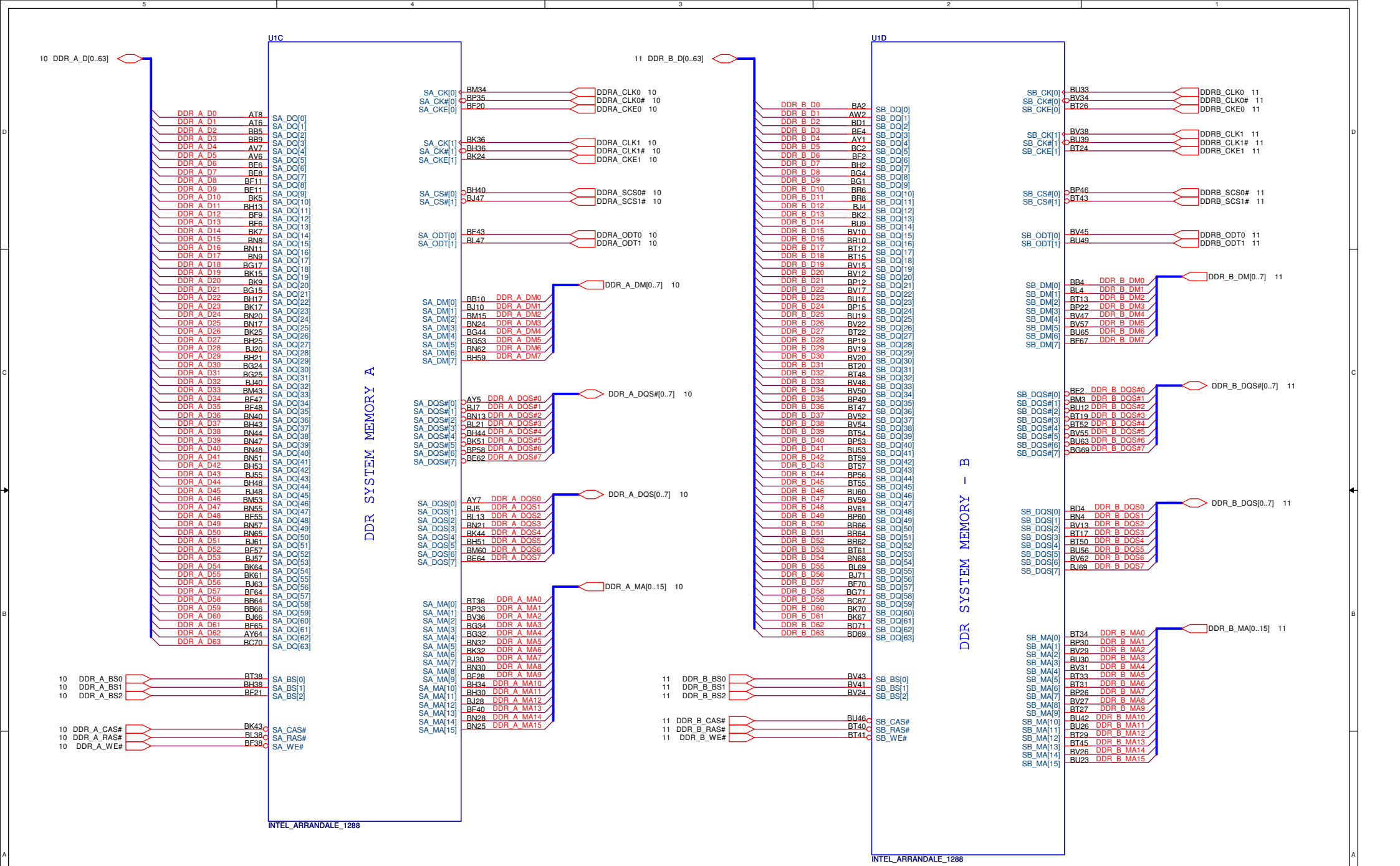
ES1 sample need negative voltage  
ES2 sample contact to GND

CFG4-Display Port Presence

CFG4 1: Disabled; No Physical Display Port attached to Embedded Display Port  
0: Enabled; An external Display Port device is connected to the Embedded Display Port

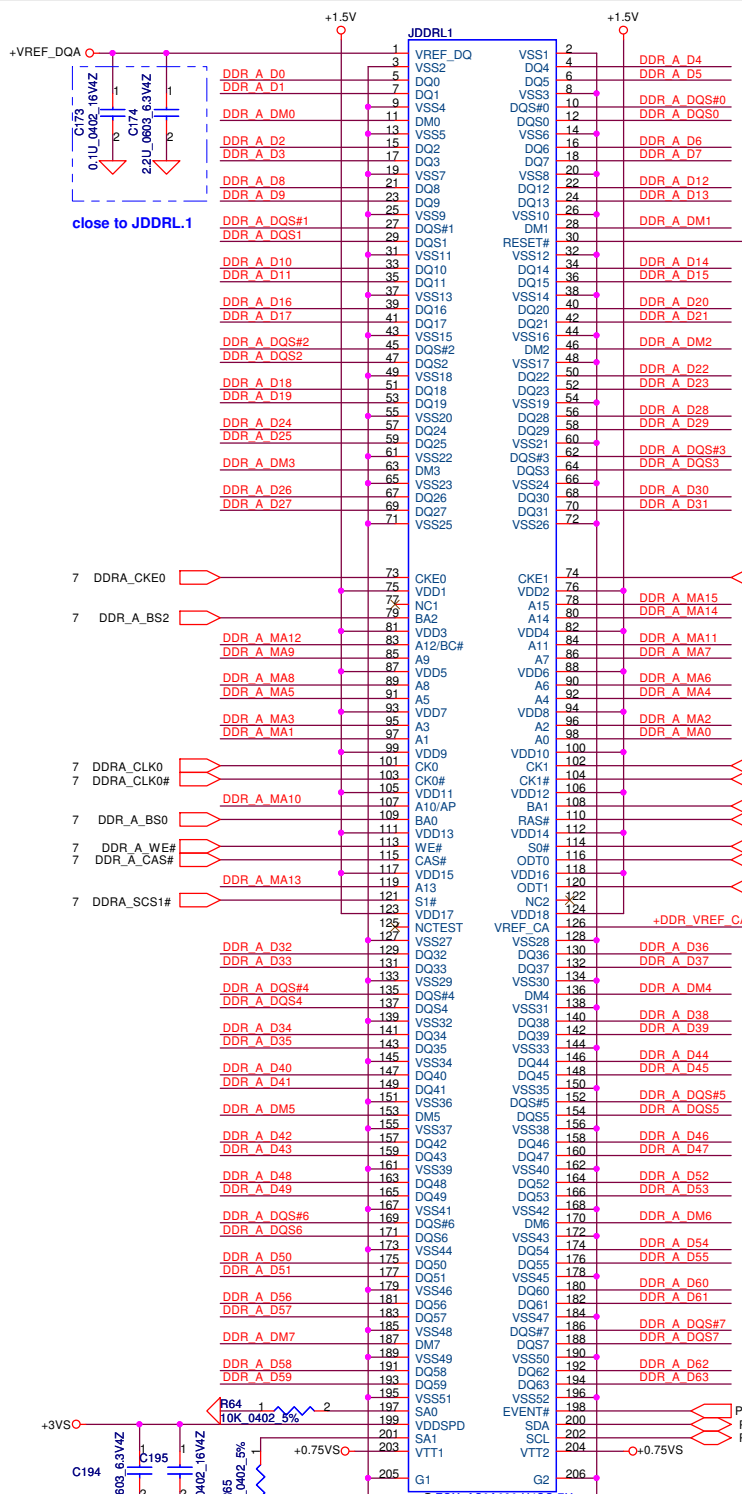


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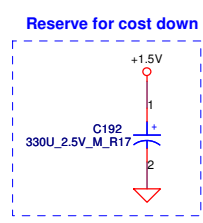
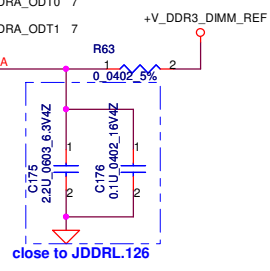
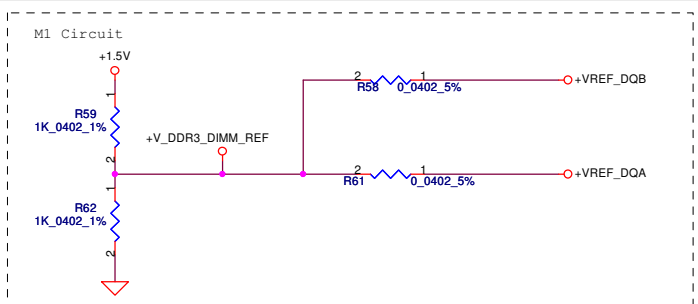
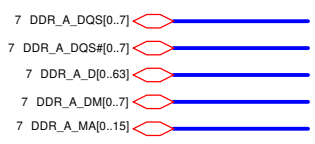




U11		AY24		U1J	
BU62	VSS1	VSS90		AH93	VSS202
BU68	VSS2	VSS91	AY23	AH91	VSS203
BU69	VSS3	VSS92	AY21	AH92	VSS204
BU65	VSS4	VSS93	AY19	AH93	VSS205
BU61	VSS5	VSS94	AY17	AH94	VSS206
BU48	VSS6	VSS95	AY15	AH95	VSS207
BU44	VSS7	VSS96	AY14	AH96	VSS208
BU37	VSS8	VSS97	AY12	AH97	VSS209
BU32	VSS9	VSS98	AY10	AH98	VSS210
BU25	VSS10	VSS99	AY4	AH99	VSS211
BU18	VSS11	VSS100	AW67	AH100	VSS212
BU14	VSS12	VSS101	AW62	AH101	VSS213
BU11	VSS13	VSS102	AW59	AH102	VSS214
BU7	VSS14	VSS103	AW55	AH103	VSS215
BP42	VSS15	VSS104	AW48	AH104	VSS216
BP42	VSS16	VSS105	AW44	AH105	VSS217
BP42	VSS17	VSS106	AW41	AH106	VSS218
BP42	VSS18	VSS107	AW37	AH107	VSS219
BP42	VSS19	VSS108	AW32	AH108	VSS220
BP42	VSS20	VSS109	AW28	AH109	VSS221
BP42	VSS21	VSS110	AW24	AH110	VSS222
BP42	VSS22	VSS111	AW20	AH111	VSS223
BP42	VSS23	VSS112	AW16	AH112	VSS224
BP42	VSS24	VSS113	AW12	AH113	VSS225
BP42	VSS25	VSS114	AW08	AH114	VSS226
BP42	VSS26	VSS115	AW04	AH115	VSS227
BP42	VSS27	VSS116	AW00	AH116	VSS228
BP42	VSS28	VSS117	AW00	AH117	VSS229
BP42	VSS29	VSS118	AW00	AH118	VSS230
BP42	VSS30	VSS119	AW00	AH119	VSS231
BP42	VSS31	VSS120	AW00	AH120	VSS232
BP42	VSS32	VSS121	AW00	AH121	VSS233
BP42	VSS33	VSS122	AW00	AH122	VSS234
BP42	VSS34	VSS123	AW00	AH123	VSS235
BP42	VSS35	VSS124	AW00	AH124	VSS236
BP42	VSS36	VSS125	AW00	AH125	VSS237
BP42	VSS37	VSS126	AW00	AH126	VSS238
BP42	VSS38	VSS127	AW00	AH127	VSS239
BP42	VSS39	VSS128	AW00	AH128	VSS240
BP42	VSS40	VSS129	AW00	AH129	VSS241
BP42	VSS41	VSS130	AW00	AH130	VSS242
BP42	VSS42	VSS131	AW00	AH131	VSS243
BP42	VSS43	VSS132	AW00	AH132	VSS244
BP42	VSS44	VSS133	AW00	AH133	VSS245
BP42	VSS45	VSS134	AW00	AH134	VSS246
BP42	VSS46	VSS135	AW00	AH135	VSS247
BP42	VSS47	VSS136	AW00	AH136	VSS248
BP42	VSS48	VSS137	AW00	AH137	VSS249
BP42	VSS49	VSS138	AW00	AH138	VSS250
BP42	VSS50	VSS139	AW00	AH139	VSS251
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BP42	VSS55	VSS144	AW00	AH144	VSS256
BP42	VSS56	VSS145	AW00	AH145	VSS257
BP42	VSS57	VSS146	AW00	AH146	VSS258
BP42	VSS58	VSS147	AW00	AH147	VSS259
BP42	VSS59	VSS148	AW00	AH148	VSS260
BP42	VSS60	VSS149	AW00	AH149	VSS261
BP42	VSS61	VSS150	AW00	AH150	VSS262
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BP42	VSS63	VSS152	AW00	AH152	VSS264
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BP42	VSS65	VSS154	AW00	AH154	VSS266
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BP42	VSS67	VSS156	AW00	AH156	VSS268
BP42	VSS68	VSS157	AW00	AH157	VSS269
BP42	VSS69	VSS158	AW00	AH158	VSS270
BP42	VSS70	VSS159	AW00	AH159	VSS271
BP42	VSS71	VSS160	AW00	AH160	VSS272
BP42	VSS72	VSS161	AW00	AH161	VSS273
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BP42	VSS79	VSS168	AW00	AH168	VSS280
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BP42	VSS81	VSS170	AW00	AH170	VSS282
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BP42	VSS83	VSS172	AW00	AH172	VSS284
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BP42	VSS149	VSS238	AW00	AH238	VSS350
BP42	VSS150	VSS239	AW00	AH239	VSS351
BP42	VSS151	VSS240	AW00	AH240	VSS352
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BP42	VSS168	VSS257	AW00	AH257	VSS369
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BP42	VSS170	VSS259	AW00	AH259	VSS371
BP42	VSS171	VSS260	AW00	AH260	VSS372
BP42	VSS172	VSS261	AW00	AH261	VSS373
BP42	VSS173	VSS262	AW00	AH262	VSS374
BP42	VSS174	VSS263	AW00	AH263	VSS375
BP42	VSS175	VSS264	AW00	AH264	VSS376
BP42	VSS176	VSS265	AW00	AH265	VSS377
BP42	VSS177	VSS266	AW00	AH266	VSS378
BP42	VSS178	VSS267	AW00	AH267	VSS379
BP42	VSS179	VSS268	AW00	AH268	VSS380
BP42	VSS180	VSS269	AW00	AH269	VSS381
BP42	VSS181	VSS270	AW00	AH270	VSS382
BP42	VSS182	VSS271	AW00	AH271	VSS383
BP42	VSS183	VSS272	AW00	AH272	VSS384
BP42	VSS184	VSS273	AW00	AH273	VSS385
BP42	VSS185	VSS274	AW00	AH274	VSS386
BP42	VSS186	VSS275	AW00	AH275	VSS387
BP42	VSS187	VSS276	AW00	AH276	VSS388
BP42	VSS188	VSS277	AW00	AH277	VSS389
BP42	VSS189	VSS278	AW00	AH278	VSS390
BP42	VSS190	VSS279	AW00	AH279	VSS391
BP42	VSS191	VSS280	AW00	AH280	VSS392
BP42	VSS192	VSS281	AW00	AH281	VSS393
BP42	VSS193	VSS282	AW00	AH282	VSS394
BP42	VSS194	VSS283	AW00	AH283	VSS395
BP42	VSS195	VSS284	AW00	AH284	VSS396
BP42	VSS196	VSS285	AW00	AH285	VSS397
BP42	VSS197	VSS286	AW00	AH286	VSS398
BP42	VSS198	VSS287	AW00	AH287	VSS399
BP42	VSS199	VSS288	AW00	AH288	VSS400
BP42	VSS200	VSS289	AW00	AH289	VSS401
BP42	VSS201	VSS290	AW00	AH290	VSS402
BP42	VSS202	VSS291	AW00	AH291	VSS403
BP42	VSS203	VSS292	AW00	AH292	VSS404
BP42	VSS204	VSS293	AW00	AH293	VSS405
BP42	VSS205	VSS294	AW00	AH294	VSS406
BP42	VSS206	VSS295	AW00	AH295	VSS407
BP42	VSS207	VSS296	AW00	AH296	VSS408
BP42	VSS208	VSS297	AW00	AH297	VSS409
BP42	VSS209	VSS298	AW00	AH298	VSS410
BP42	VSS210	VSS299	AW00	AH299	VSS411
BP42	VSS211	VSS300	AW00	AH300	VSS412
BP42	VSS212	VSS301	AW00	AH301	VSS413
BP42	VSS213	VSS302	AW00	AH302	VSS414
BP42	VSS214	VSS303	AW00	AH303	VSS415
BP42	VSS215	VSS304	AW00	AH304	VSS416
BP42	VSS216	VSS305	AW00	AH305	VSS417
BP42	VSS217	VSS306	AW00	AH306	VSS418
BP42	VSS218	VSS307	AW00	AH307	VSS419
BP42	VSS219	VSS308	AW00	AH308	VSS420
BP42	VSS220	VSS309	AW00	AH309	VSS421
BP42	VSS221	VSS310	AW00	AH310	VSS422
BP42	VSS222	VSS311	AW00		



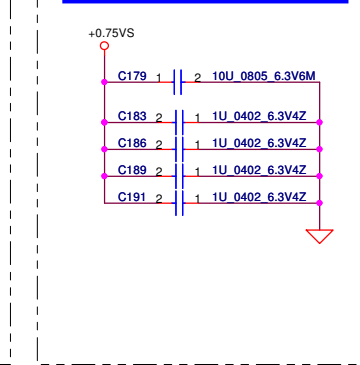
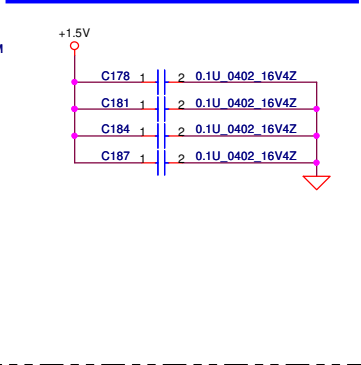
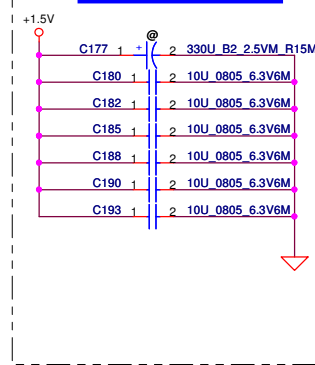
# DDR3 SO-DIMM A Standard Type



Layout Note:  
Place near JDDR1

Layout Note: Place these 4 Caps near  
Command and Control signals of DIMMA

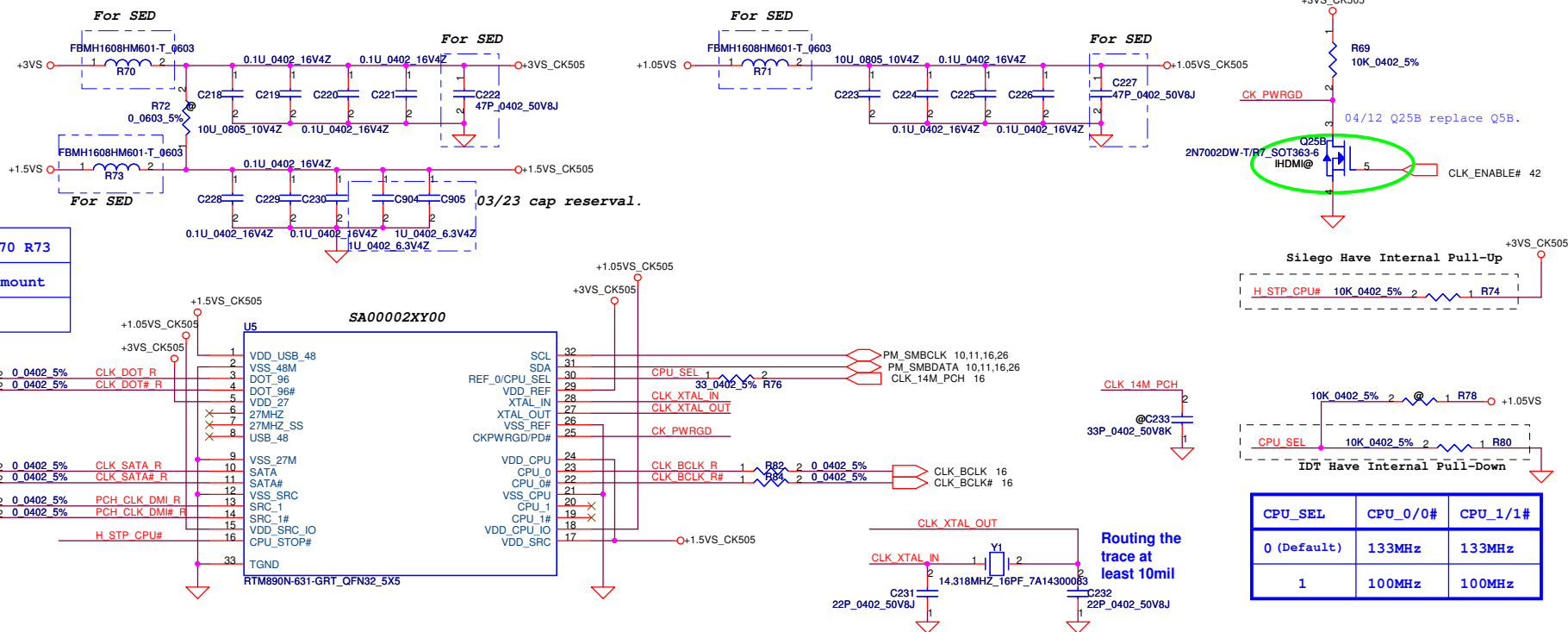
Layout Note:  
Place near JDDR1.203 and 204



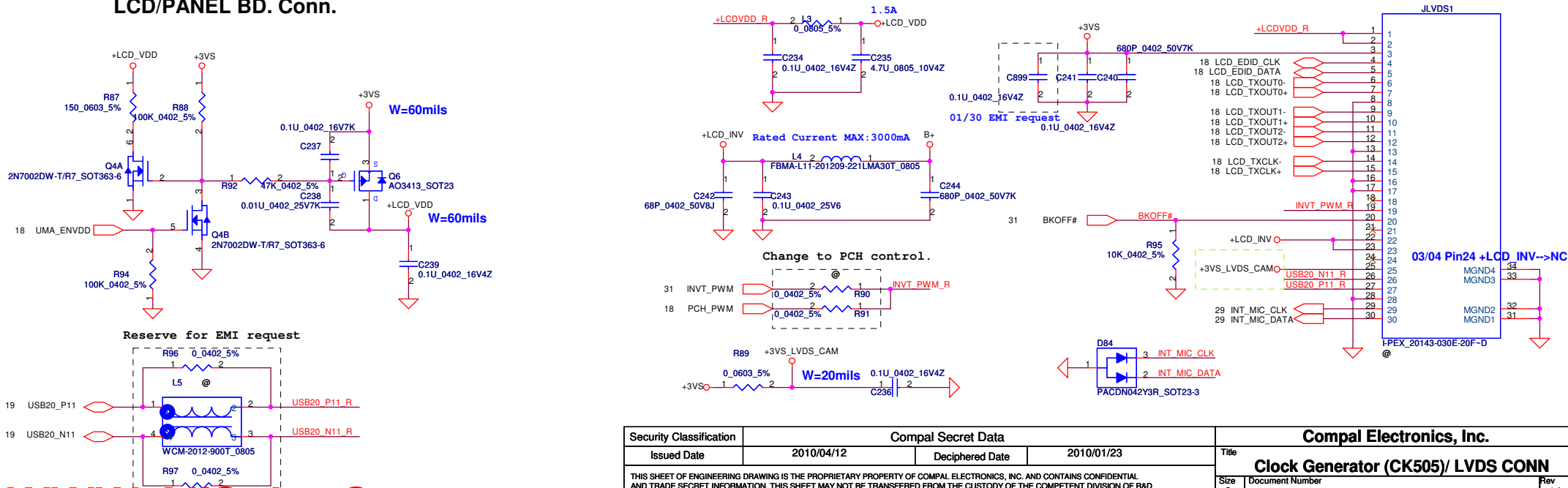
Compal Secret Data				Compal Electronics, Inc.		
Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title		
				DDRIII-SODIMMO		
				Size	Document Number	Rev
				Custom	NDU00_LA-6031P M/B	1.0
				Date:	Monday, April 12, 2010	Sheet 10 of 45



## Clock Generator

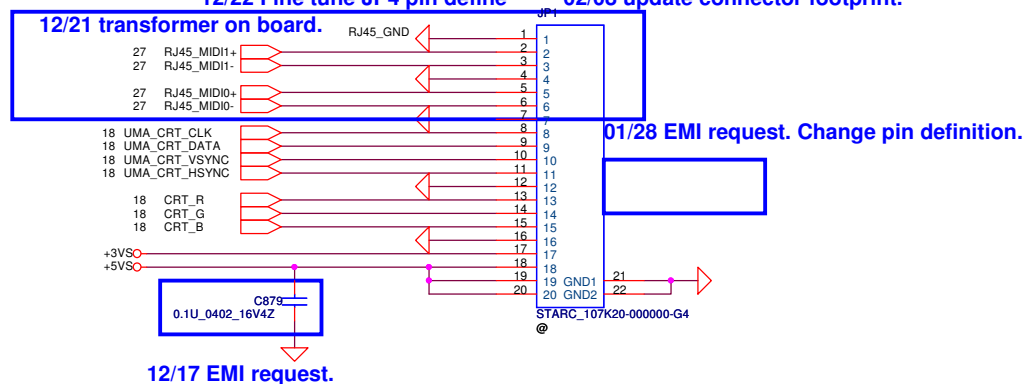


**LCD/PANEL BD. Conn.**



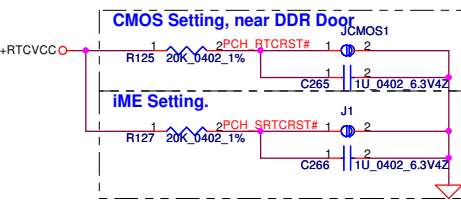
# CRT CONNECTOR

12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND  
12/21 pin 2,3 to RJ45\_GND  
12/22 Fine tune JP4 pin define 02/08 update connector footprint.



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Size		Document Number			Rev
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**Integrated SUS 1.05V VRM Enable**

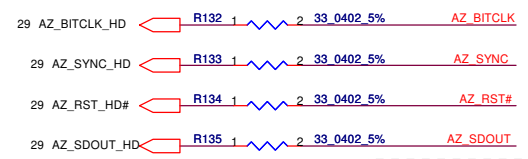
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

**HDA\_SYNC**  
This signal has a weak internal pull down.  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
This signal has a weak internal pull down.  
This signal can't PU

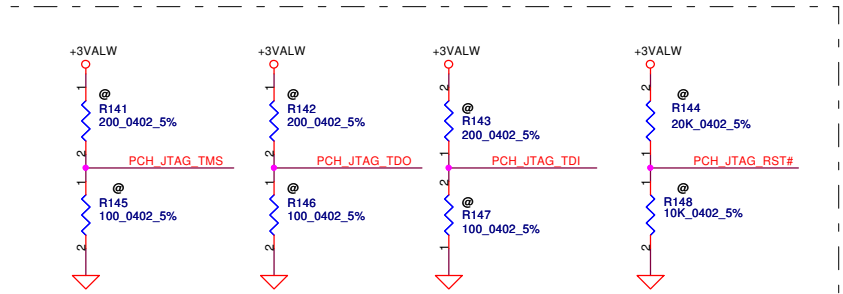
**Flash Descriptor Security Override**

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



**ITPM Enabled Internal: Pull down 20k**

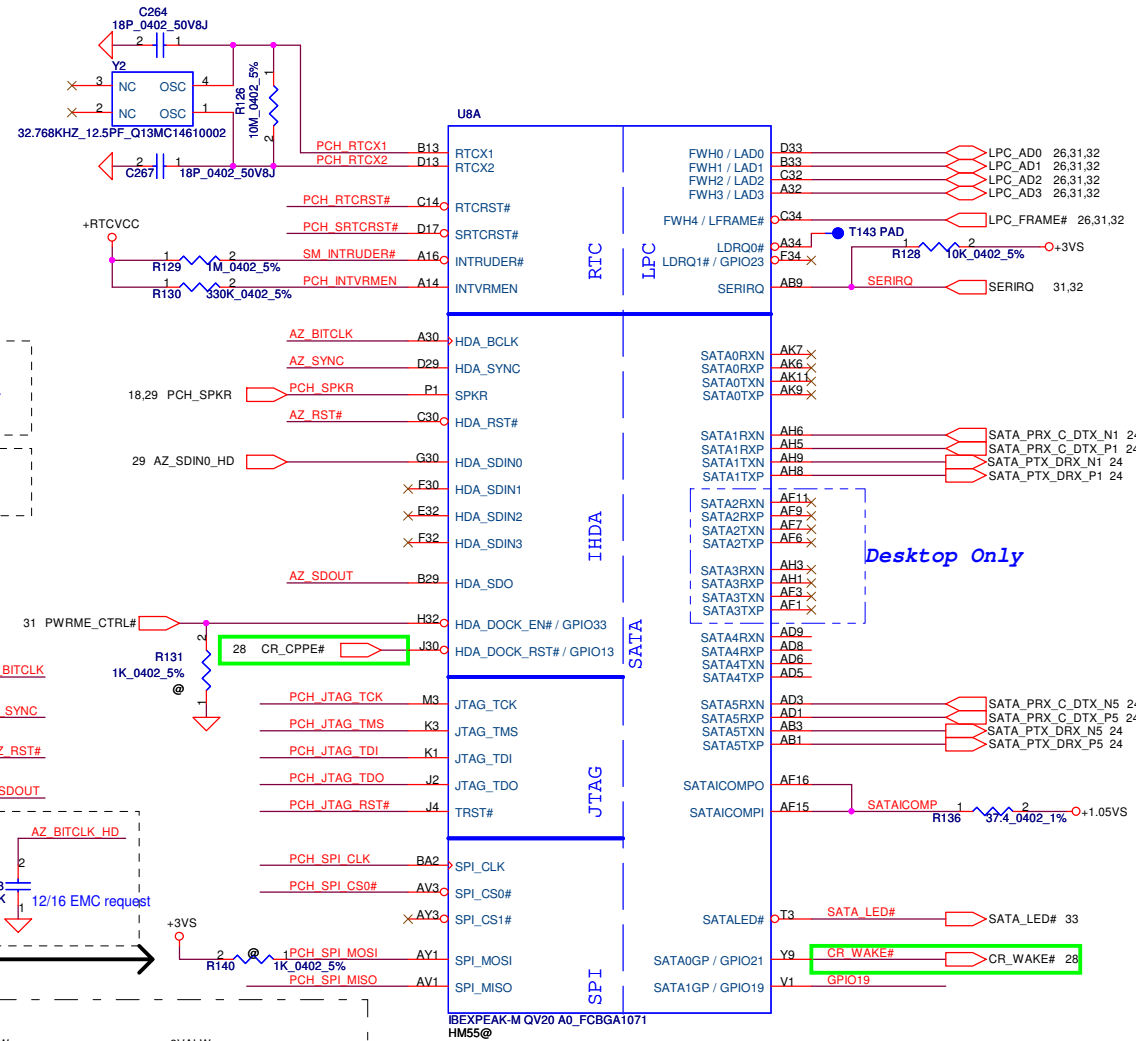
SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



06/01 change R125 from 4.7K to 51 ohm

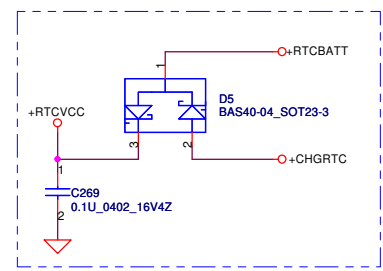
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDO	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TDI	R357	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_TCK	R156	51ohm	51ohm	No Install	No Install

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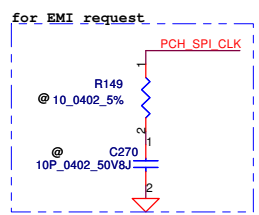
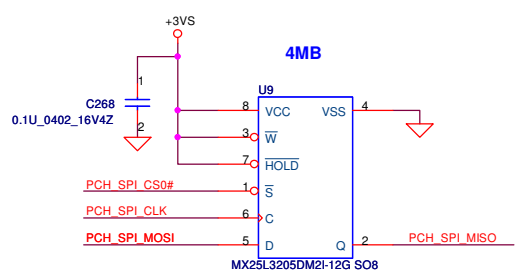
1ST HDD

eSATA

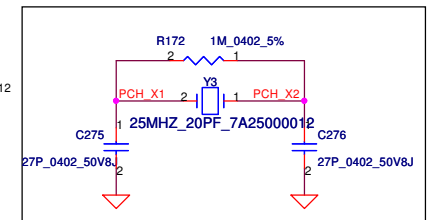
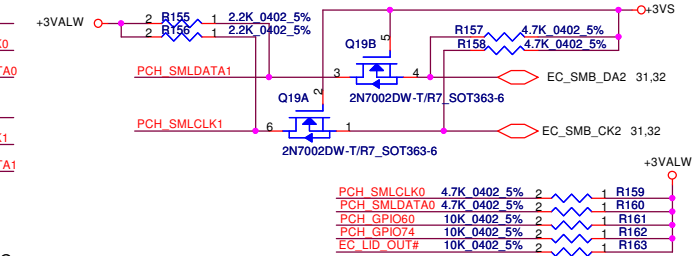



2/8 change back to original.(Lion Wang)  
del D86 and R1494.

2/1 Add R1494 D86 (EMI)

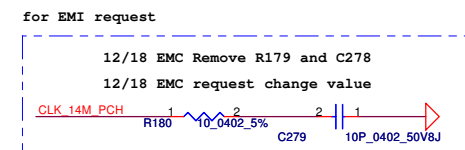


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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								<b>PCH-SPI/SATA/LPC/RTC/HDA</b>			
Size		Document Number						Rev			
B								NDU00_LA-6031P M/B			
Date:		Monday, April 12, 2010		Sheet		15		of 45			



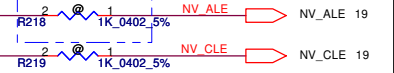
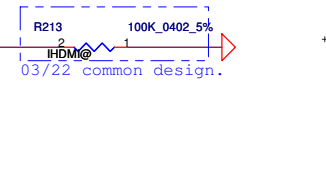
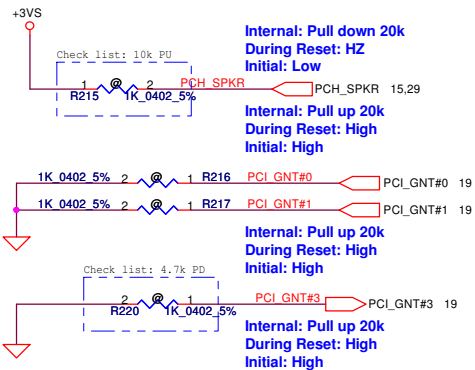
 C277 @  
0\_0402\_5%

Note: Stuff 0 ohm if  
25MHz crystal un-stuff



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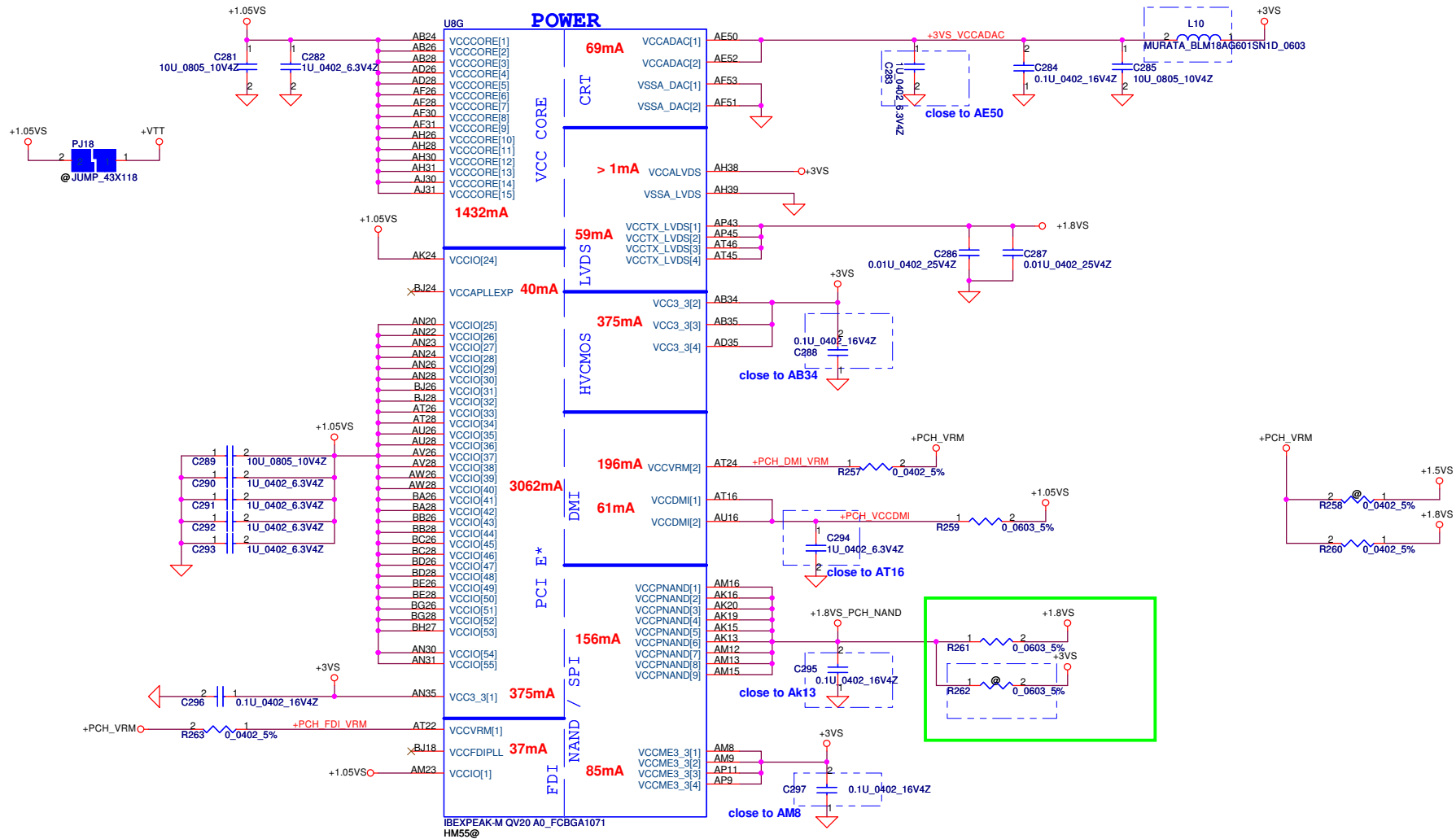
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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				NDU00_LA-6031P M/B	
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				Sheet	21 of 45
				Rev	1.0



U8I			
AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BC12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH0	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D61	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
F8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK38
H38	VSS[257]	VSS[357]	AV14
H42	VSS[258]	VSS[358]	

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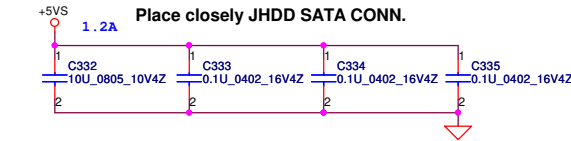
U8H			
AB16	VSS[0]		
AA19	VSS[1]	VSS[80]	AK30
AA20	VSS[2]	VSS[81]	AK31
AA22	VSS[3]	VSS[82]	AK32
AM19	VSS[4]	VSS[83]	AK34
AA24	VSS[5]	VSS[84]	AK35
AA26	VSS[6]	VSS[85]	AK38
AA28	VSS[7]	VSS[86]	AK43
AA30	VSS[8]	VSS[87]	AK46
AA31	VSS[9]	VSS[88]	AK49
AA32	VSS[10]	VSS[89]	AK5
AB11	VSS[11]	VSS[90]	AK8
AB15	VSS[12]	VSS[91]	AL2
AB23	VSS[13]	VSS[92]	AL52
AB30	VSS[14]	VSS[93]	AM11
AB31	VSS[15]	VSS[94]	BB44
AB32	VSS[16]	VSS[95]	AD24
AB39	VSS[17]	VSS[96]	AM20
AB43	VSS[18]	VSS[97]	AM22
AB47	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB5	VSS[21]	VSS[100]	AM28
AC3	VSS[22]	VSS[101]	BA42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AL20
AL22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
AD49	VSS[35]	VSS[114]	AM7
AD7	VSS[36]	VSS[115]	AA50
AE2	VSS[37]	VSS[116]	BB10
AE4	VSS[38]	VSS[117]	AN32
AF12	VSS[39]	VSS[118]	AN50
Y13	VSS[40]	VSS[119]	AN52
AA49	VSS[41]	VSS[120]	AP12
AF35	VSS[42]	VSS[121]	AP42
AP13	VSS[43]	VSS[122]	AP46
AN34	VSS[44]	VSS[123]	AP49
AF45	VSS[45]	VSS[124]	AP5
AF46	VSS[46]	VSS[125]	AP8
AF49	VSS[47]	VSS[126]	AP2
AF5	VSS[48]	VSS[127]	AP52
AF8	VSS[49]	VSS[128]	AT11
AG2	VSS[50]	VSS[129]	AT12
AG52	VSS[51]	VSS[130]	AT32
AH11	VSS[52]	VSS[131]	AT36
AH15	VSS[53]	VSS[132]	AT41
AH16	VSS[54]	VSS[133]	AT47
AH24	VSS[55]	VSS[134]	AT7
AH32	VSS[56]	VSS[135]	AV12
AV18	VSS[57]	VSS[136]	AV16
AH43	VSS[58]	VSS[137]	AV20
AH47	VSS[59]	VSS[138]	AV24
AH7	VSS[60]	VSS[139]	AV30
AI19	VSS[61]	VSS[140]	AV34
AI2	VSS[62]	VSS[141]	AV38
AI20	VSS[63]	VSS[142]	AV42
AI26	VSS[64]	VSS[143]	AV46
AI22	VSS[65]	VSS[144]	AV49
AI23	VSS[66]	VSS[145]	AV5
AI25	VSS[67]	VSS[146]	AV8
AI28	VSS[68]	VSS[147]	AW14
AI32	VSS[69]	VSS[148]	AW18
AI34	VSS[70]	VSS[149]	AW2
AT5	VSS[71]	VSS[150]	BF9
AI4	VSS[72]	VSS[151]	AW32
AK12	VSS[73]	VSS[152]	AW36
AM41	VSS[74]	VSS[153]	AW40
AN19	VSS[75]	VSS[154]	AW52
AK26	VSS[76]	VSS[155]	AY11
AK22	VSS[77]	VSS[156]	AY43
AK23	VSS[78]	VSS[157]	AY47
AK28	VSS[79]	VSS[158]	

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				Custom	Rev
				Date:	Monday, April 12, 2010
				Sheet	23 of 45
				NDU00_LA-6031P M/B	

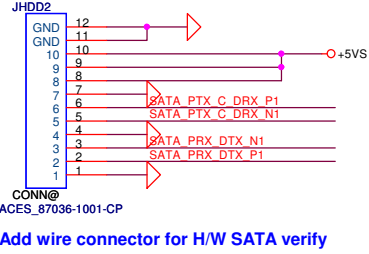
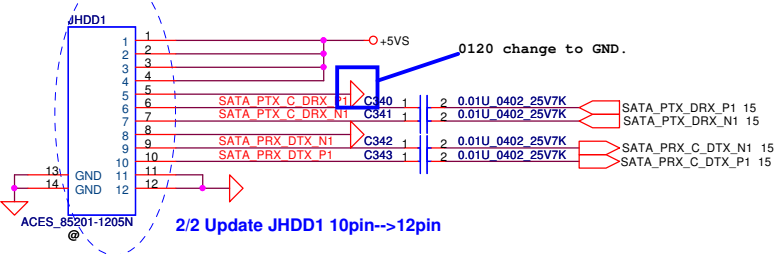
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SATA HDD Conn.



1/28 Add JHDD2

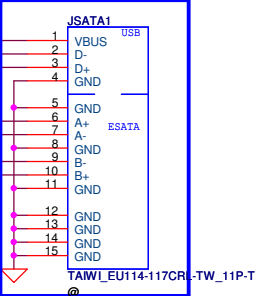
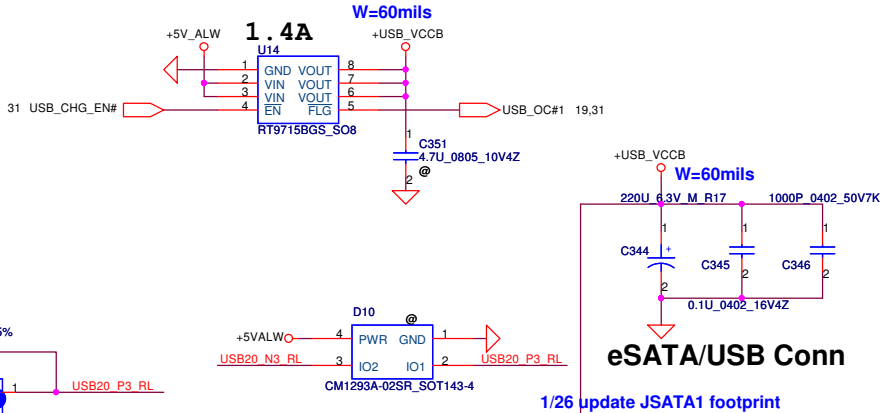
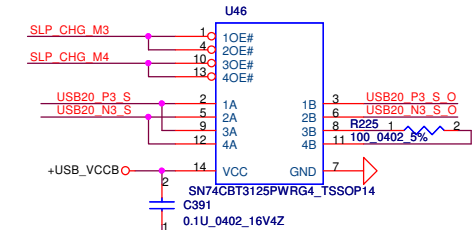
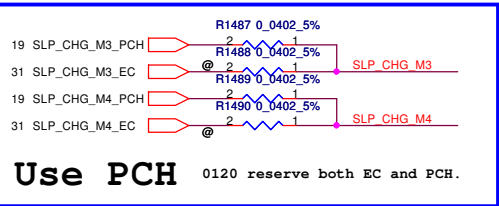
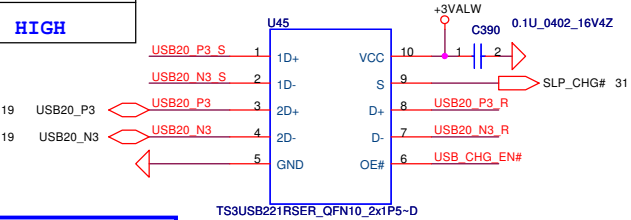
JHDD2 Layout symbol reverse JHDD1, recerse the pin define



eSATA/USB Combo

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

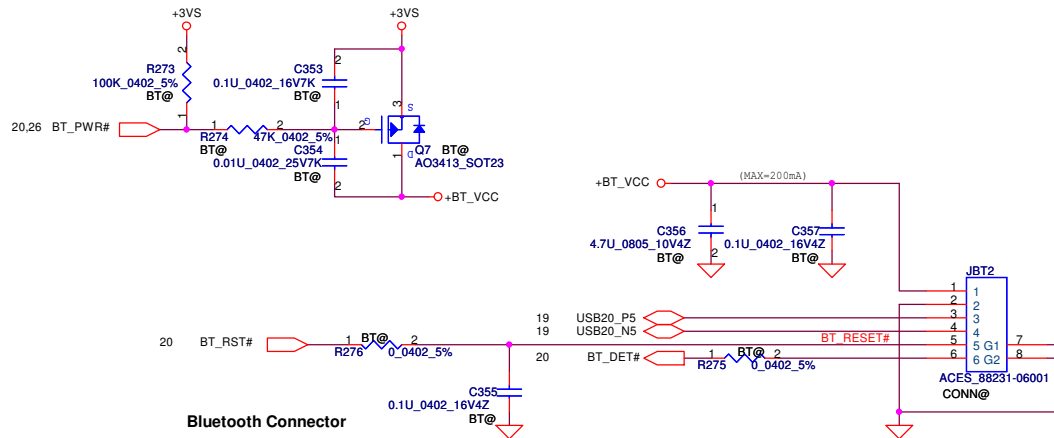
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



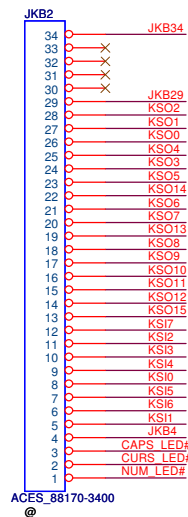
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Size		Document Number		Rev	
		NDU00_LA-6031P M/B		1.0	
Date:		Monday, April 12, 2010		Sheet 24 of 45	

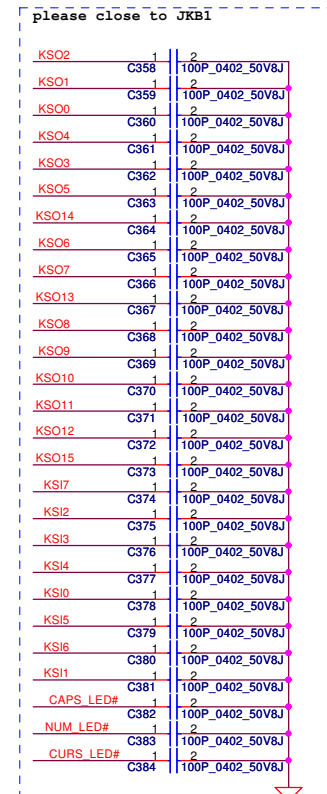
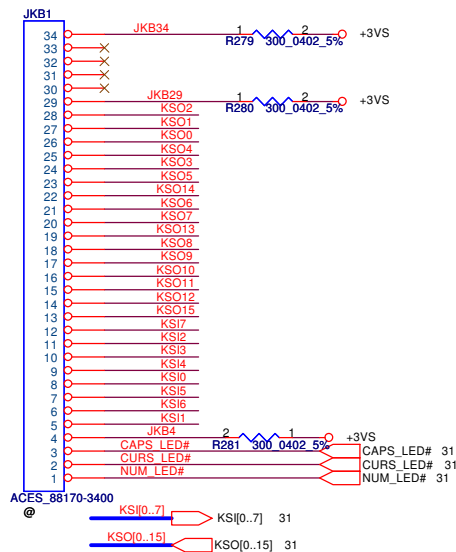
# BlueTooth Interface



## KEYBOARD CONN. for 11.6"

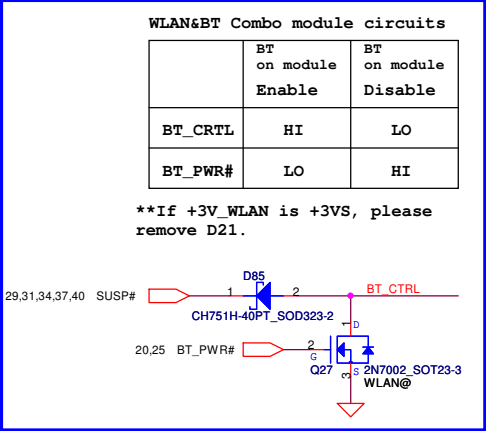


## KEYBOARD CONN. for 13.3"



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Size		Document Number		Rev	
Date		Monday, April 12, 2010		Sheet 25 of 45	
NDU00_LA-6031P M/B		1.0			

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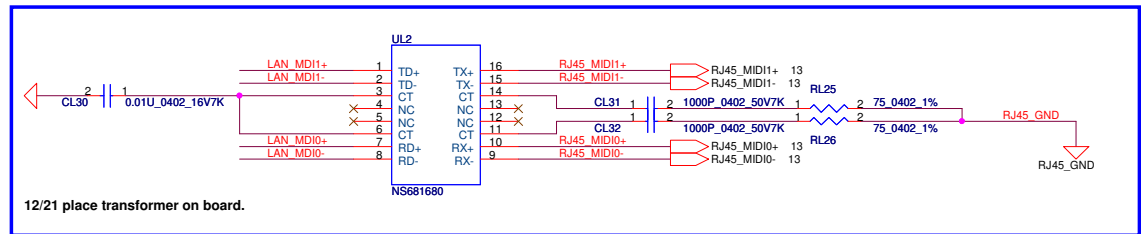
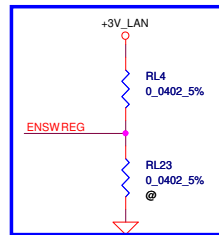
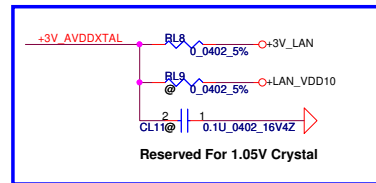
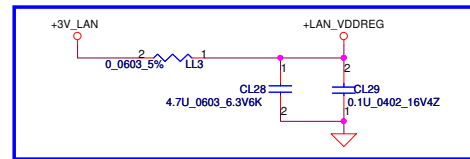
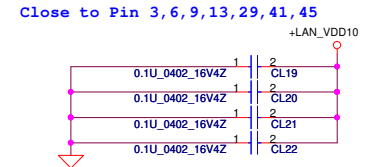
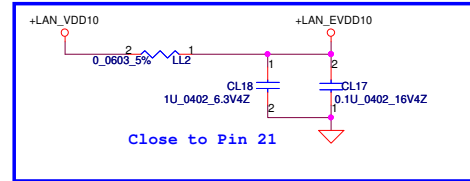
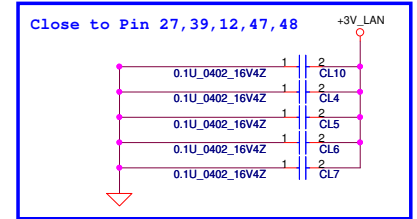
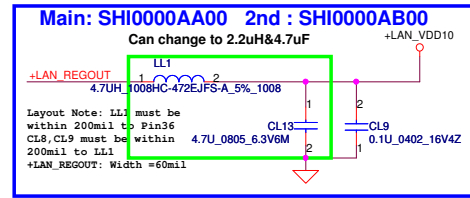
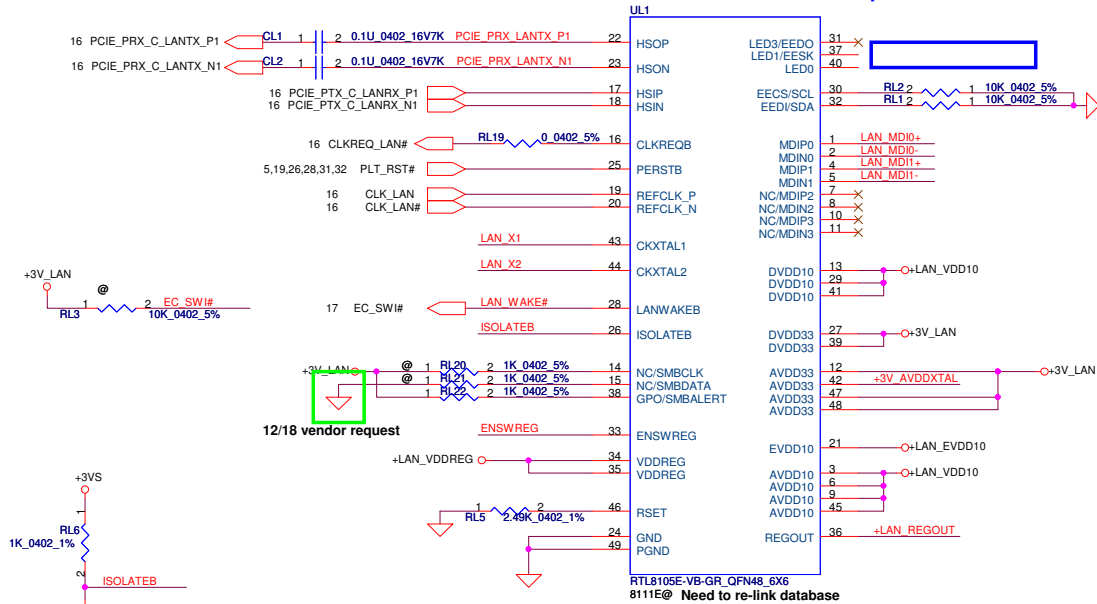


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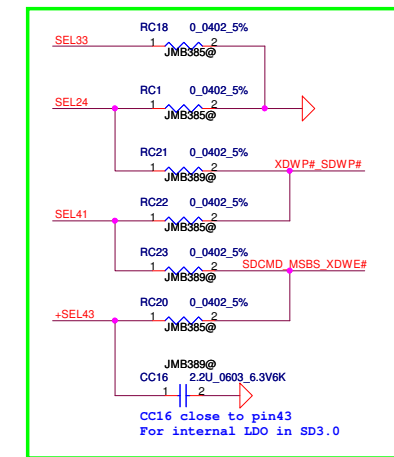
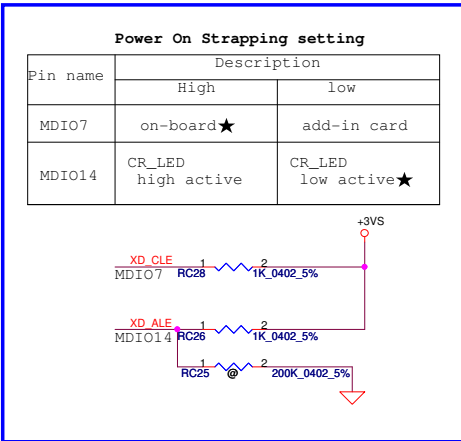
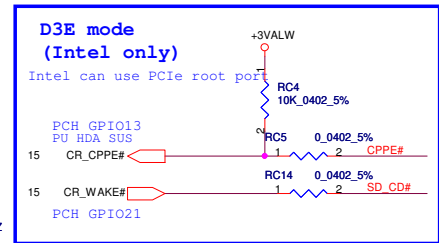
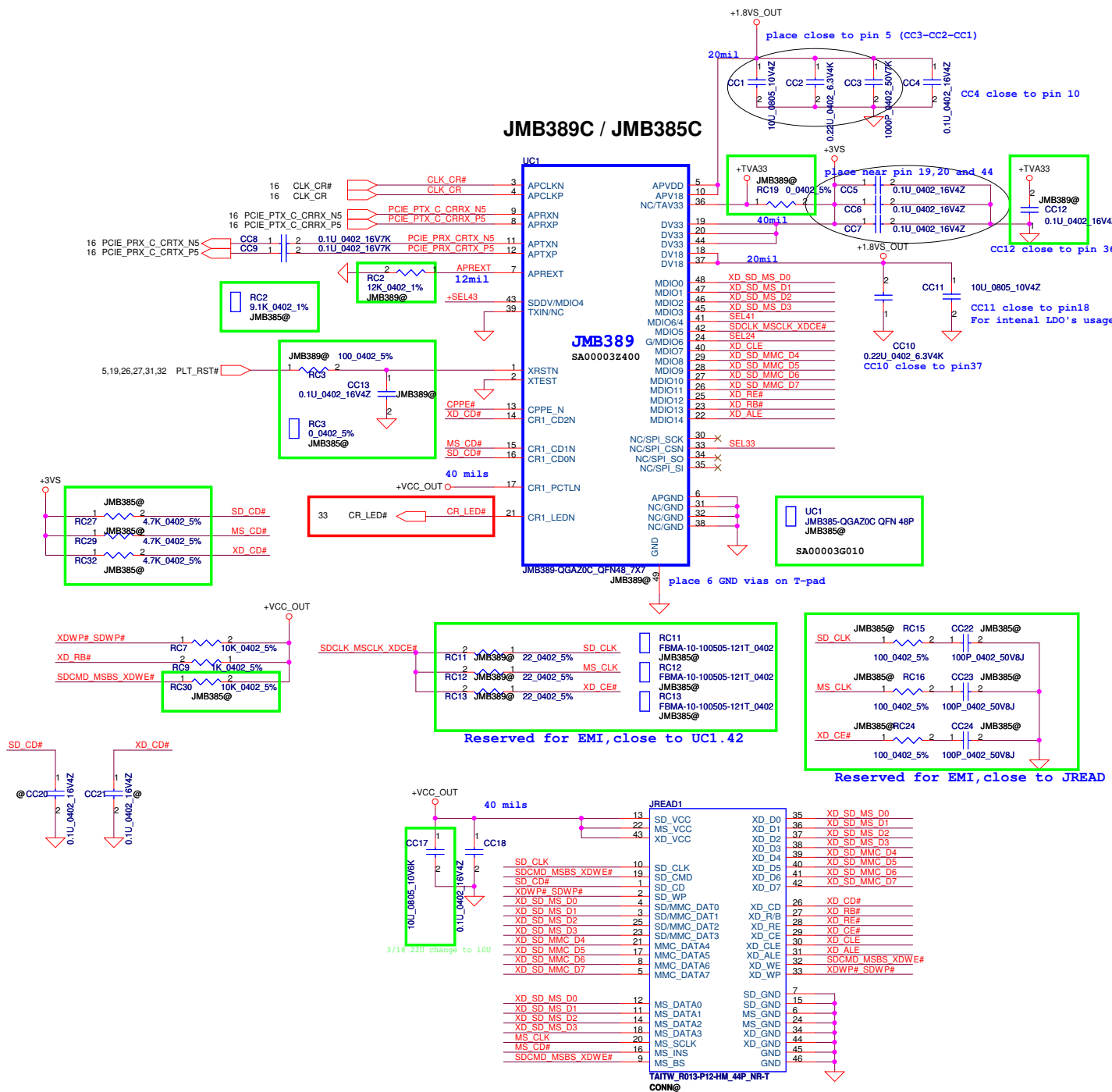
Title	PCIe-WLAN/HDDVD/NAND/NEW
-------	--------------------------

# 12/14 Fine tune pin define UL1 Pin37 Pin40 -->Dummy



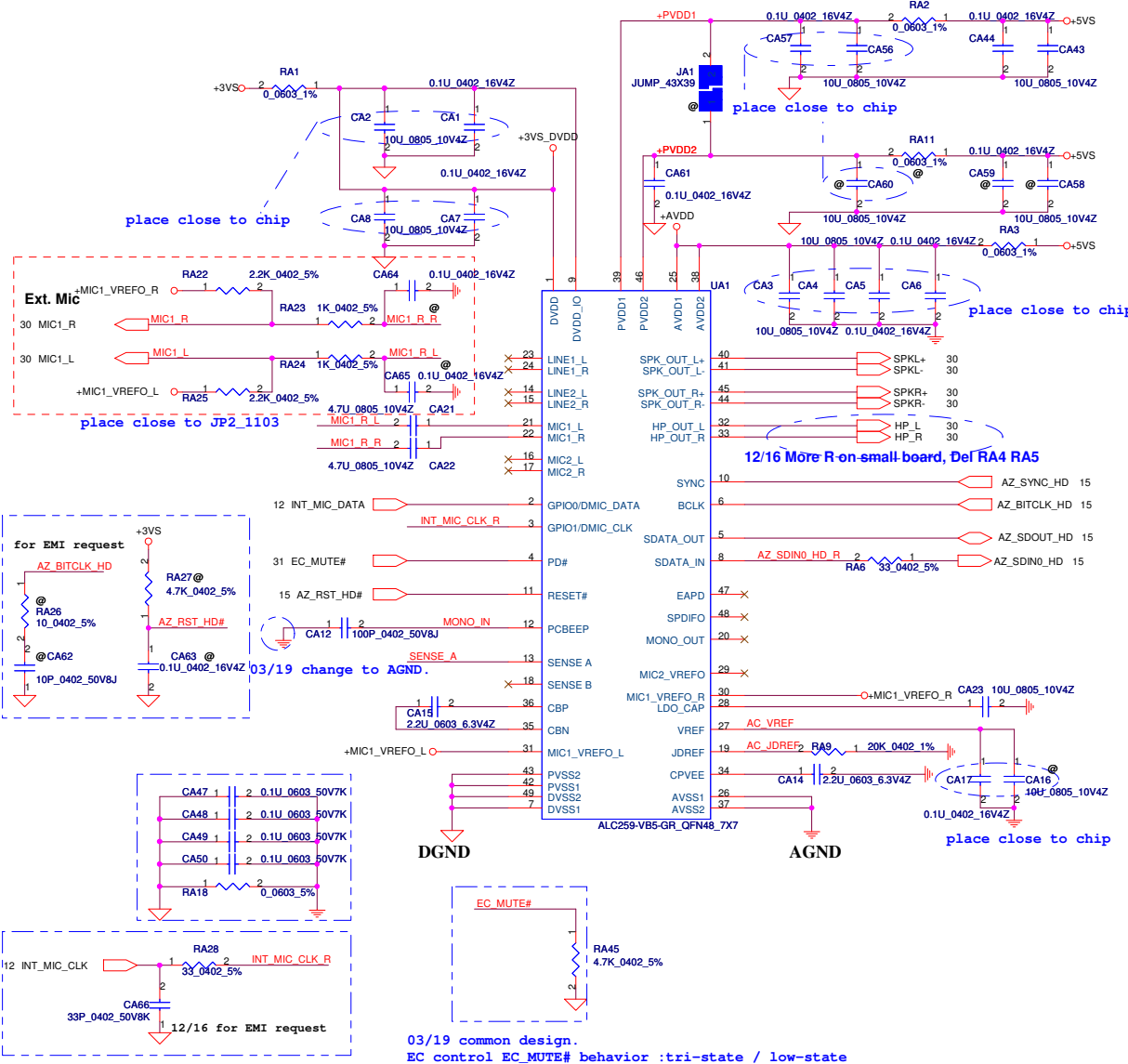
Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/12	Deciphered Date	2010/02/02	RTL8105E/RTL8111E	
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				NDU00_LA-6031P M/B	
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# JMB389C / JMB385C

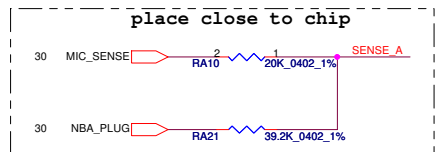


01/26 Update new card reader symbol to EVT

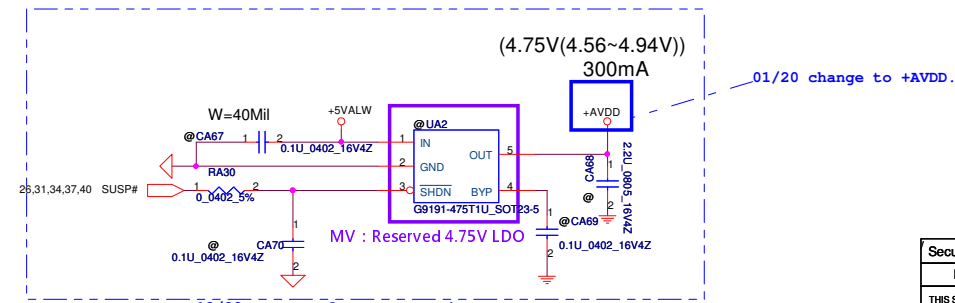
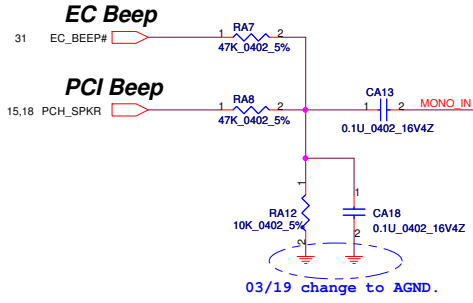
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/12	Deciphered Date	2010/10/08	Title	
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



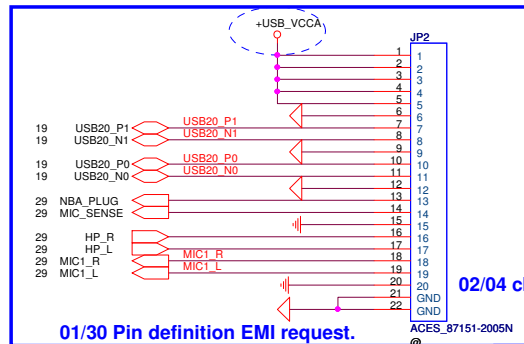
### Beep sound



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				Custom	NDU00_LA-6031P M/B
				Date	Monday, April 12, 2010
				Sheet	29 of 45

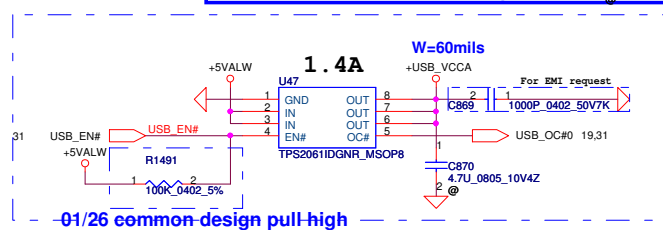
# USB+Audio FFC conn Pin=20pin, pitch=0.5

01/30 New JP2 Layout symbol reverse old conn, reverse the pin define

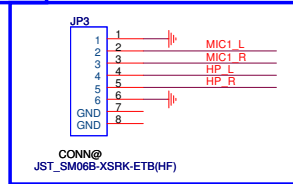


02/04 change back to 20 pins.

01/30 Pin definition EMI request.

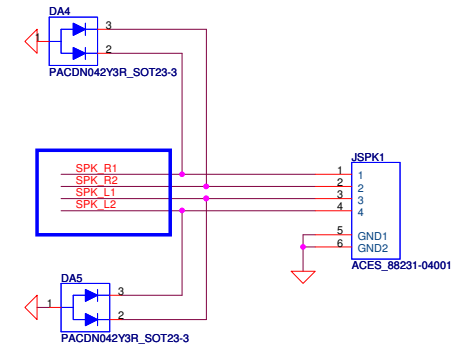
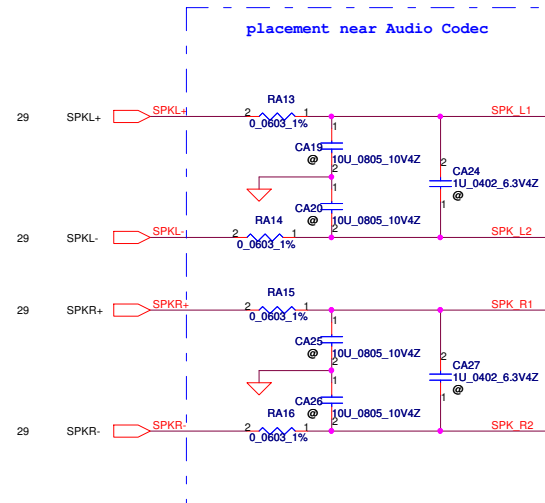


-01/26 common-design pull-high



12/19 Reserved JP6 for audio test

## Speaker Connector



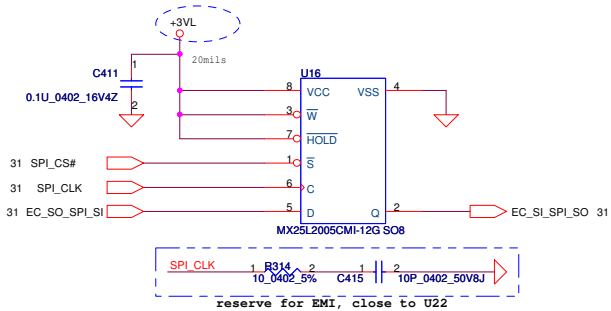
12/16 Fine tune SPK\_L1,SPK\_L2,SPK\_R1 and SPK\_R2 for SPK

Security Classification	Compal Secret Data			Title	
Issued Date	2010/04/12	Deciphered Date	2009/04/14	AMP/Audio Jack/HP/SPEAKER/VR	
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				Custom	NDU00_LA-6031P M/B
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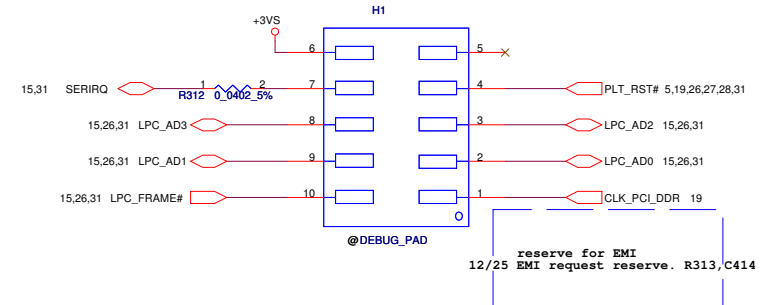
## SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

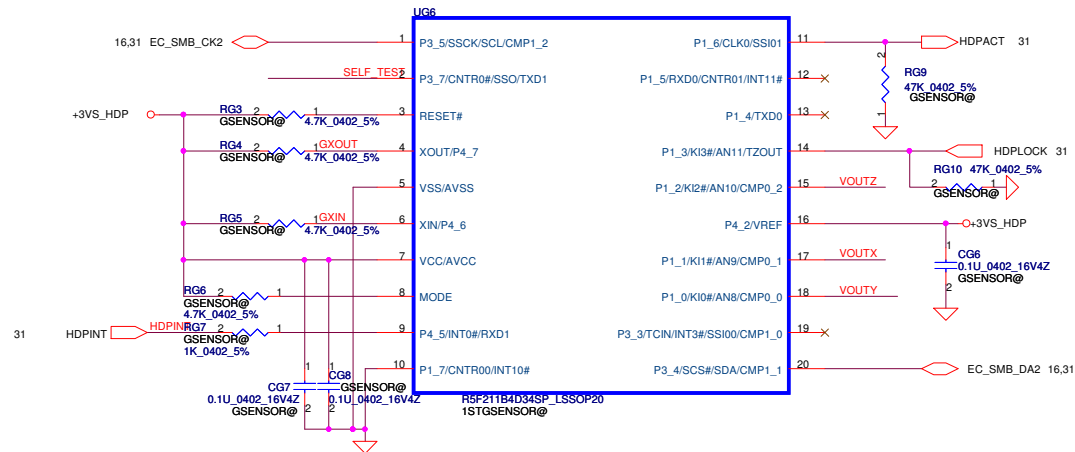
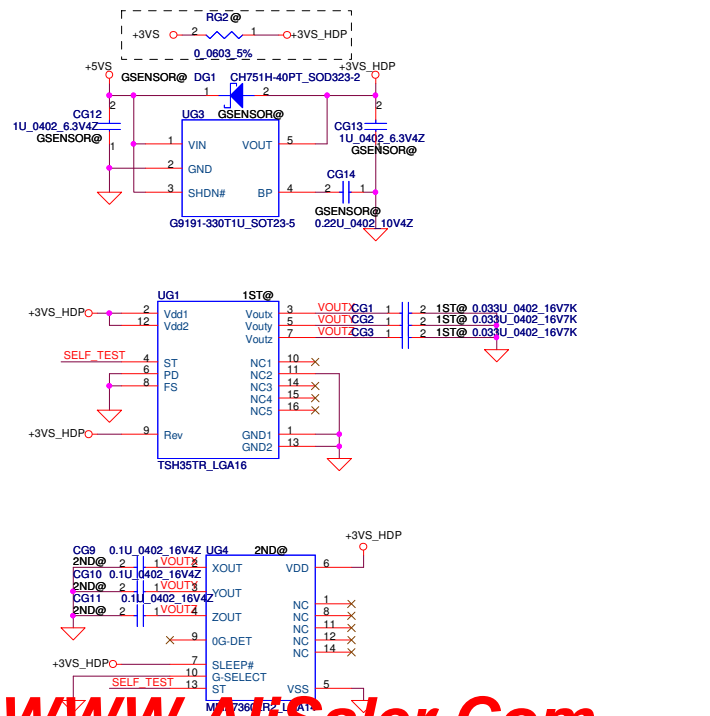


## LPC Debug Port

Please place the PAD under DDR DIMM.



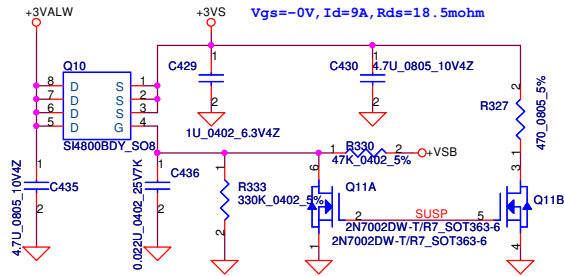
## G-Sensor



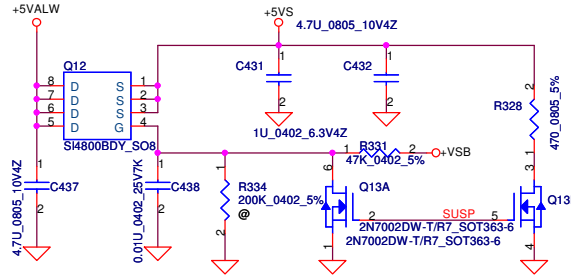
Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>						
Issued Date		2010/04/12		Deciphered Date		2009/04/14		Title				
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						Size	Document Number			<b>NDU00_LA-6031P M/B</b>		Rev 1.0
						Custor						
						Date:		Monday, April 12, 2010		Sheet	32	of



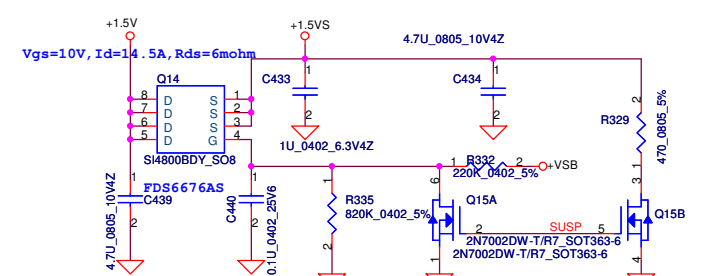
### +3VALW TO +3VS



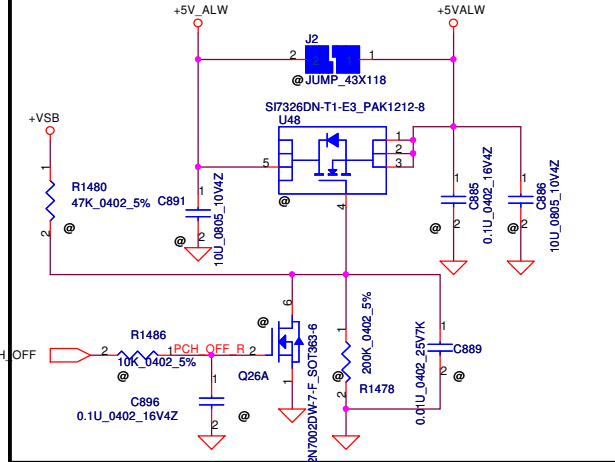
### +5VALW TO +5VS



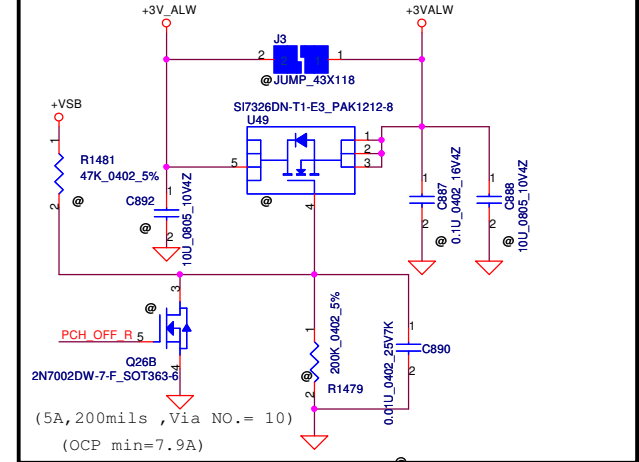
### +1.5V to +1.5VS



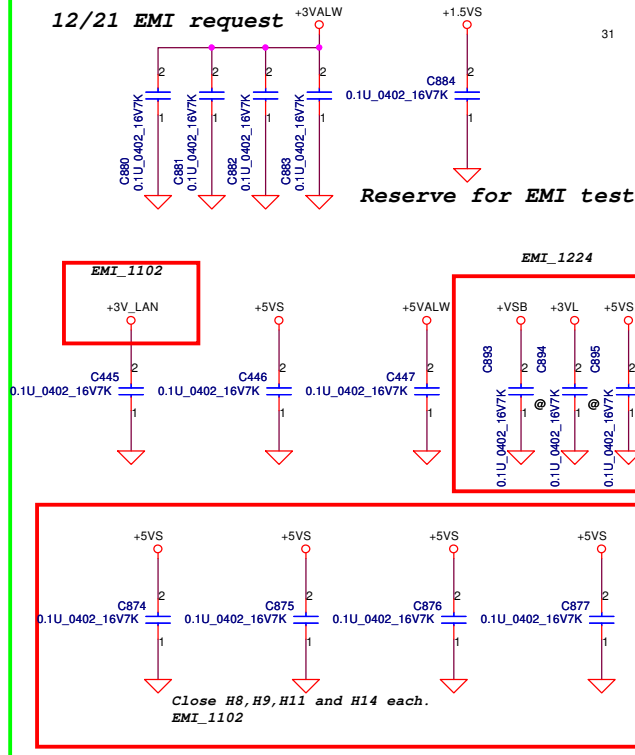
### +5V\_ALW to +5VALW Transfer



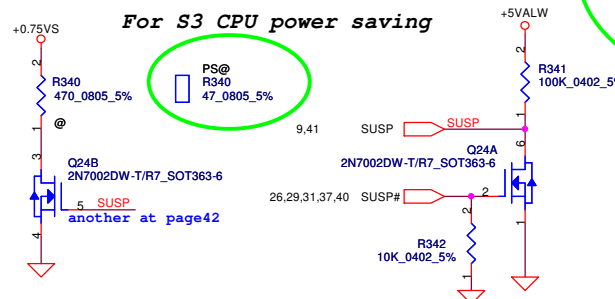
### +3V\_ALW to +3VALW Transfer



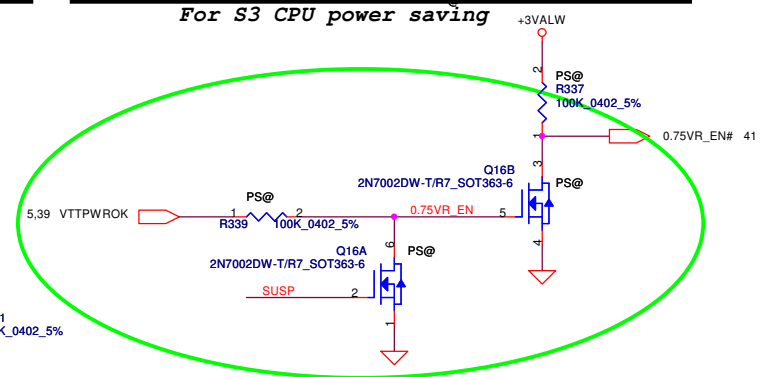
### 12/21 EMI request



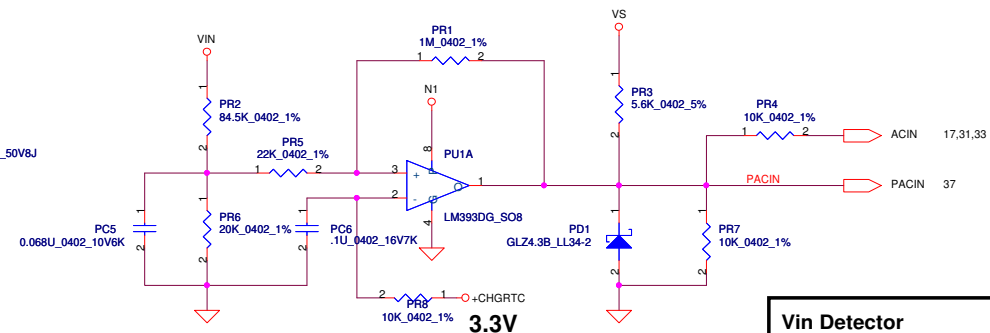
### For S3 CPU power saving



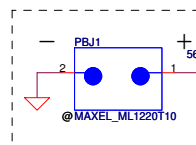
### For S3 CPU power saving



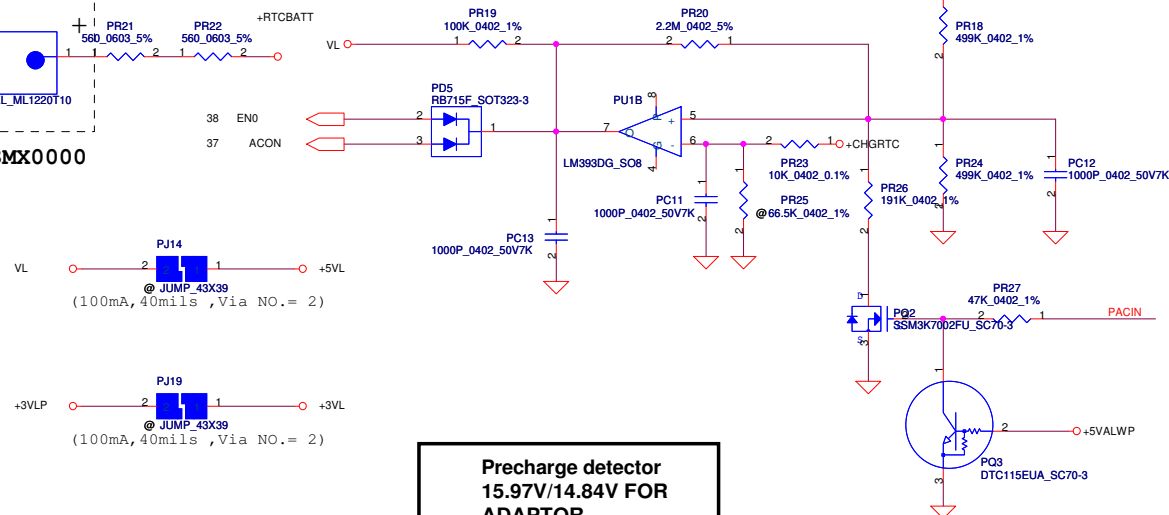
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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Size	Document Number	NDU00_LA-6031P M/B		Rev	
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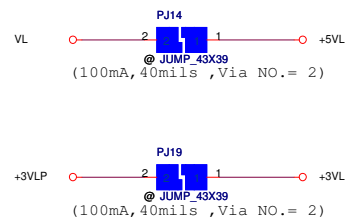
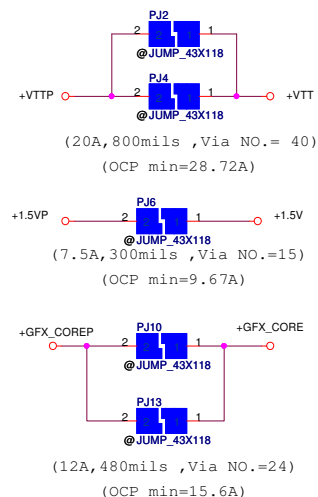
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



SP093MX0000



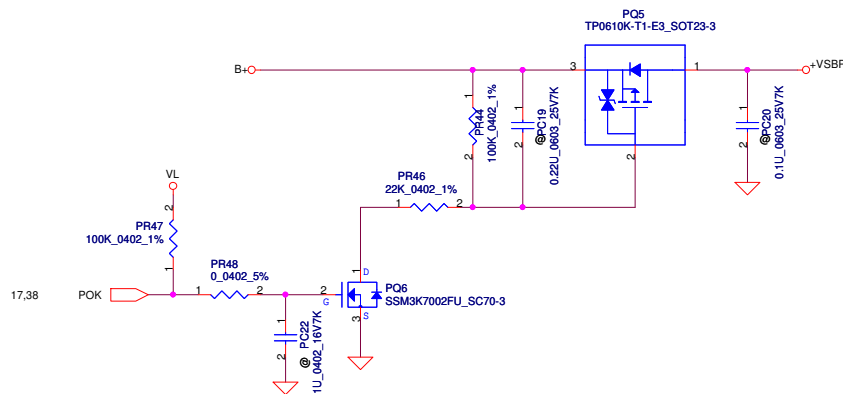
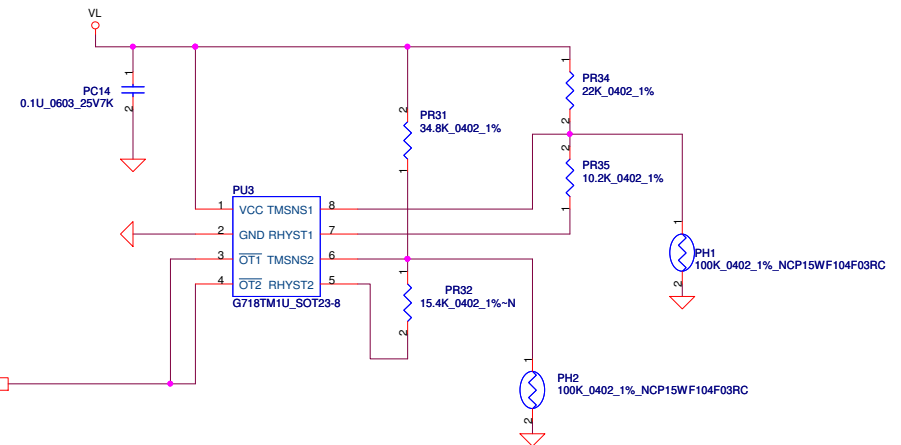
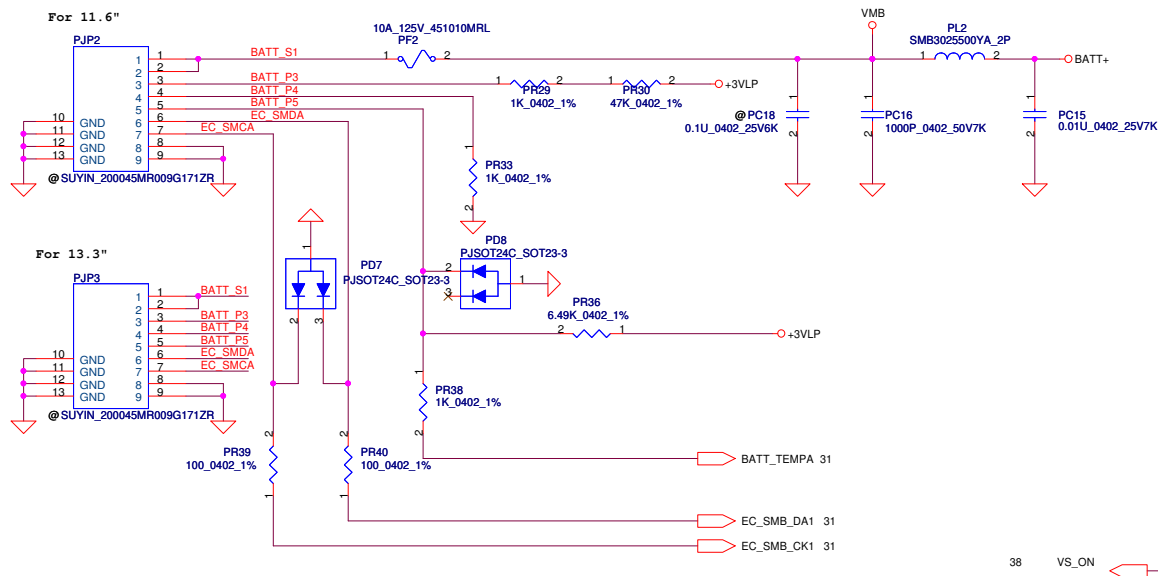
**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**



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Issued Date	2010/04/12	Deciphered Date	2010/10/02	Title DCIN / DETECTOR	
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				Date:	Monday, April 12, 2010
				Sheet	35 of 45
				Rev	1.0

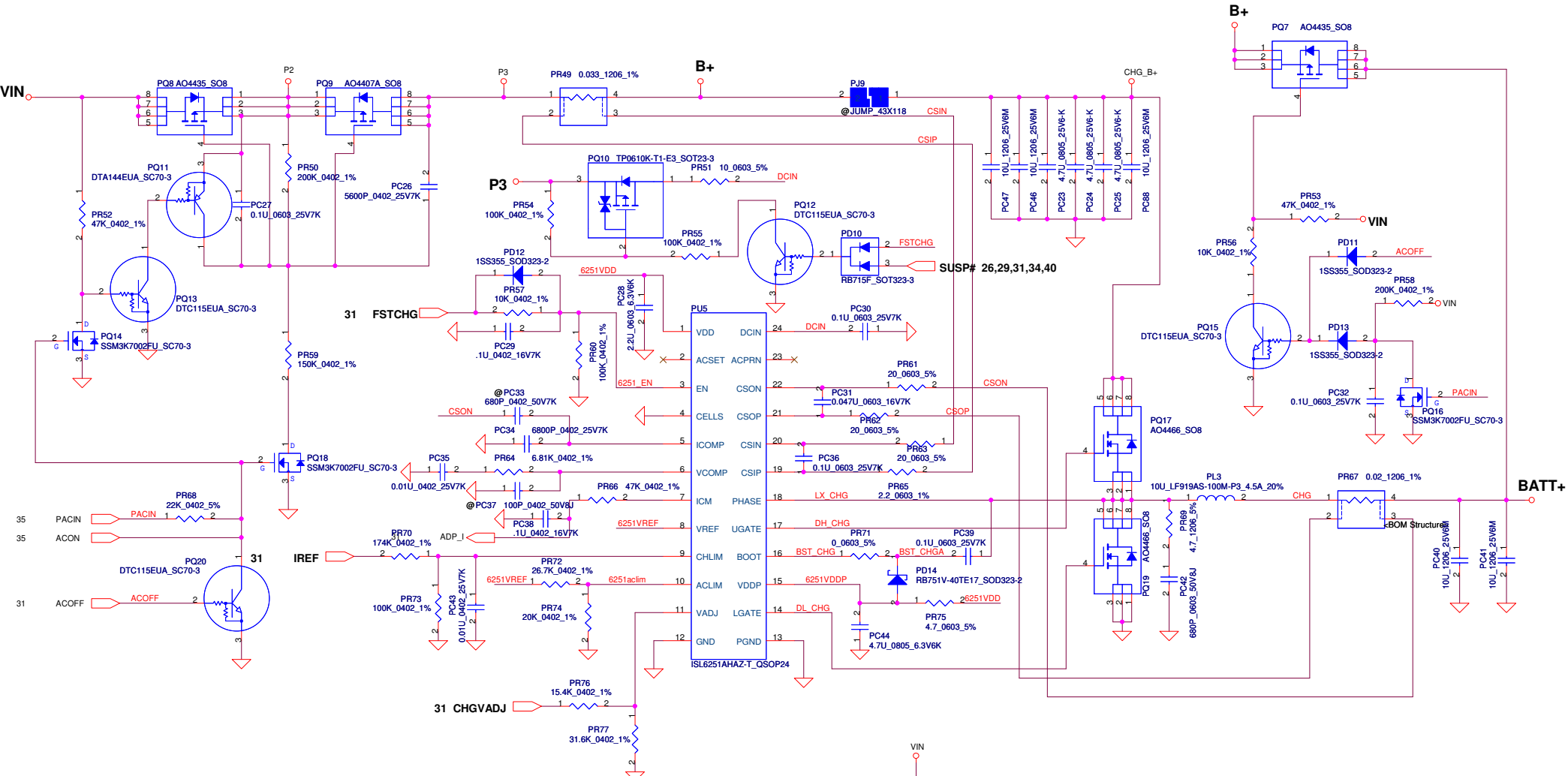
PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C

PH2 near main battery CONN:  
BAT.thermal protection at 78 degree C  
Recovery at 42 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2010/04/12		Title	
		Deciphered Date		BATTERY CONN / OTP	
		2010/10/02		Size	
				Document Number	
				LA-6031P	
				Rev	
				1.0	
				Date:	
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				36 of 45	

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$I_{ada}=0.2.368(45W)$   $CP=92\%*I_{ada}$ ;  $CP=2.178A$

CP mode  
 $V_{acim}=1.08V(65W)$   $PR72=26.7k$   $PR49=0.033$

$CC=0.25A-3A$   
 $I_{REF}=1.096*I_{charge}$   
 $I_{REF}=0.254V-3.048V$   
 $V_{CHLIM}$  need over 95mV

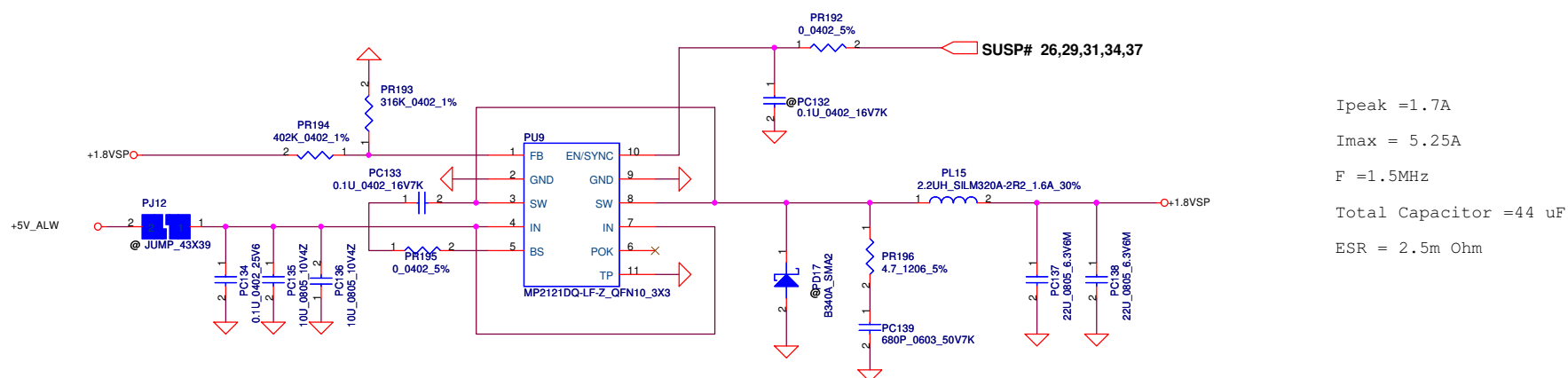
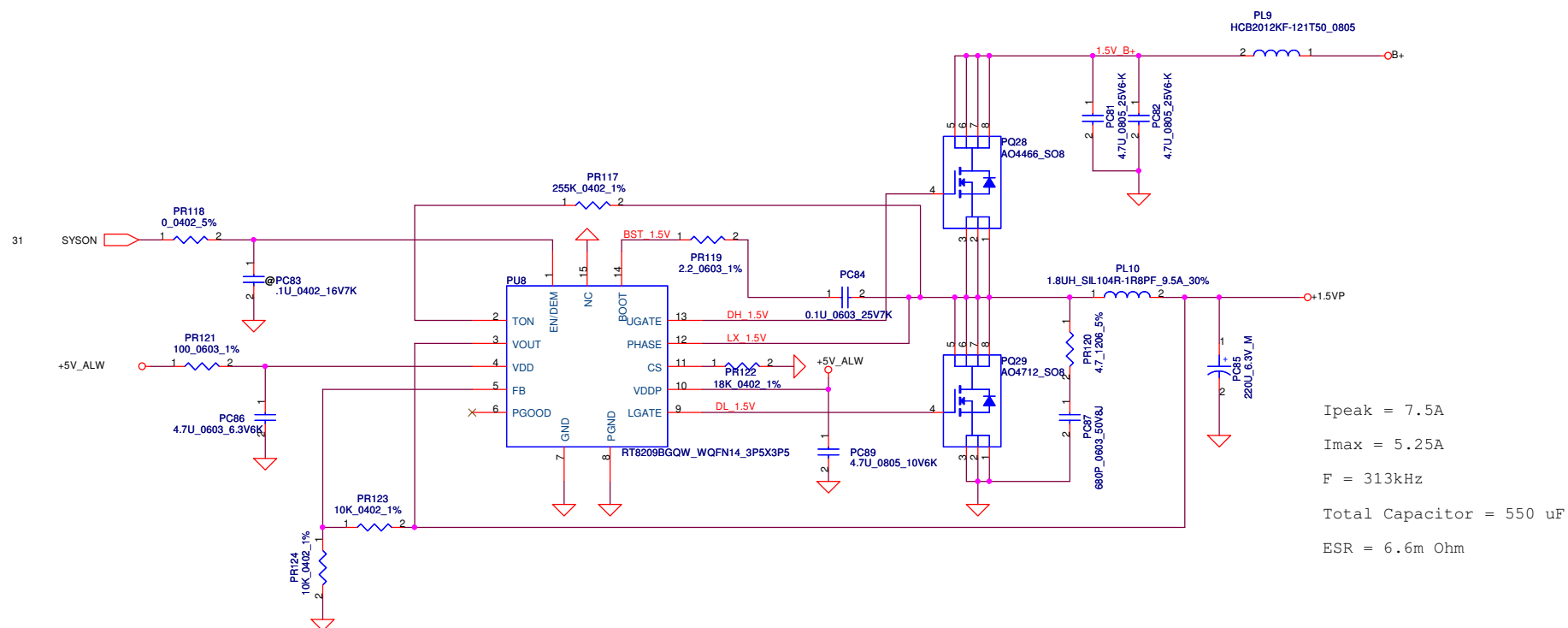
CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Ipeak = 5A  
 Imax = 3.5A  
 F = 305kHz  
 Total Capacitor = 150 uF  
 ESR = 18m Ohm

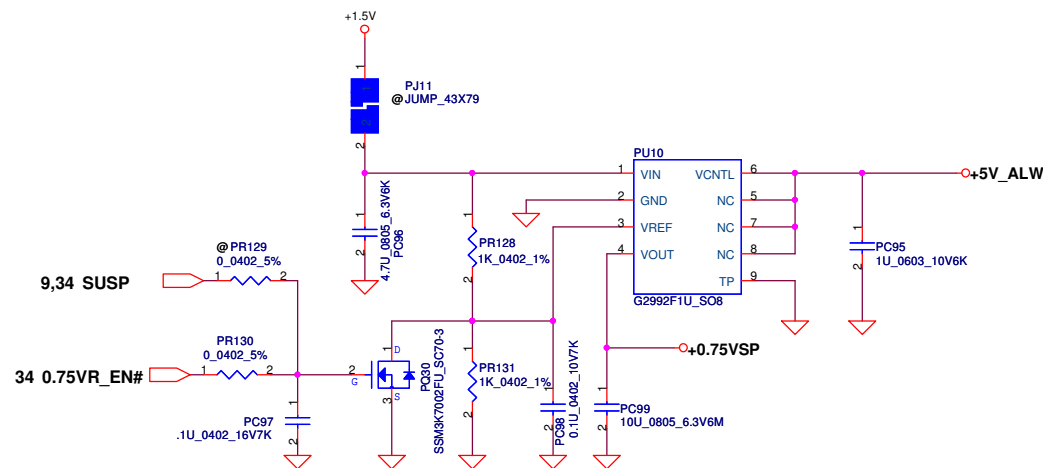
Ipeak = 5A  
 Imax = 3.5A  
 F = 245kHz  
 Total Capacitor = 150 uF  
 ESR = 18m Ohm

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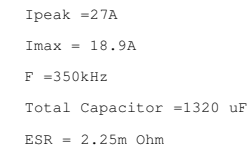


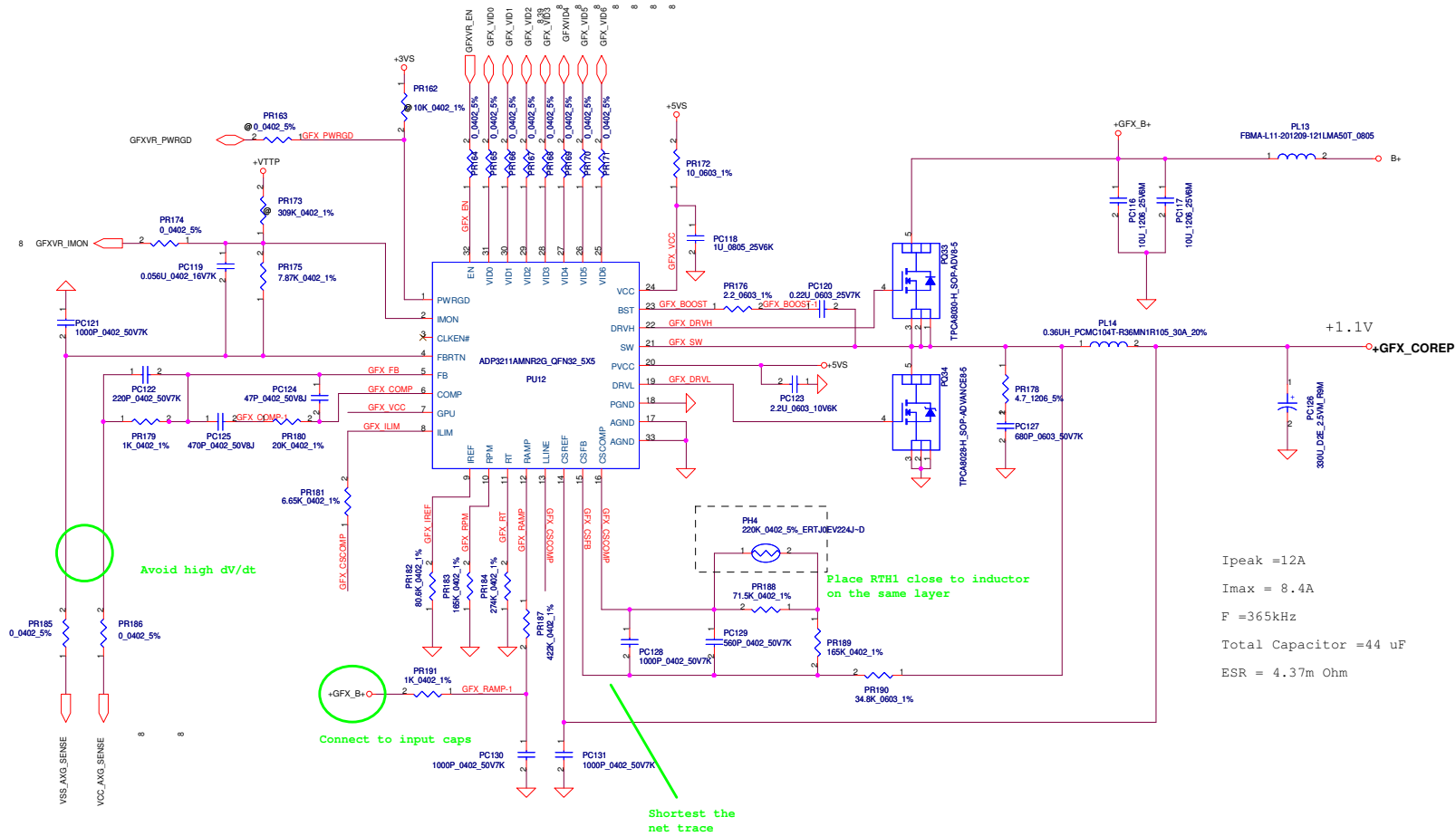


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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104KM8 to SE076104K80	change to A51 material
2009/11/9 (EVT)	P39	+VTTP	Resever PD15	Design change
2009/11/9 (EVT)	P41	+0.75VSP	Change PQ30 to SB000009610	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PU11 change to ADP3211	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PH3 &PH4	change to A51 material
2009/11/9 (EVT)	P37	CHARGE	Change PR49 change to 33m	Design change
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
2009/12/1 (DVT)	P39	+CPU-CORE	Add PR202~PR215 pull-up & pull-down	Design change
2009/12/17 (DVT)	P36	Battery	Change PR31,PR32,PR34,PR35	Design change
2009/12/17 (DVT)	P37	CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
2009/12/22 (DVT)	P42	CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P43	GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P39	+VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
2010/01/25 (PVT)	P36	Battery	Add PD7,PD8	EMI require
2010/01/27 (PVT)	P37	CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
2010/02/04 (PVT)	P41	+0.75VSP	Resever PR129 Add PR130 and PC97	Design change
2009/02/04 (PVT)	P38	+5VALWP/+3VALWP	Change PQ38	Design change
2010/02/04 (PVT)	P42	CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
2010/02/08 (PVT-2)	P36	Battery	Change PR21&PR22 and +CHGRIC	Design change

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C87 & R8, R40 and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPD circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN soft	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damage when insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add two ALW power transfer circuits (3V_ALW to 3VALW & 5V_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRS LPVR pull up 1k ohm to VIT	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SW# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24,31	Add R1487,R1488,R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change cardreader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5, and add L1C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH(U8)		layout change	03/04	PVT2
38	Change D2 to JMicon card reader.	28		03/22	PVT2
39	USB OC# change	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2

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